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35	EC+KBC	0.40	20060612				

Value	MS50/GM	MS50/PM	MS30/GM	MS30/PM
MS30_			V	V
MS50_	V	V		
CA_	V		V	
NV_		V		V
NC_	V	V	V	V

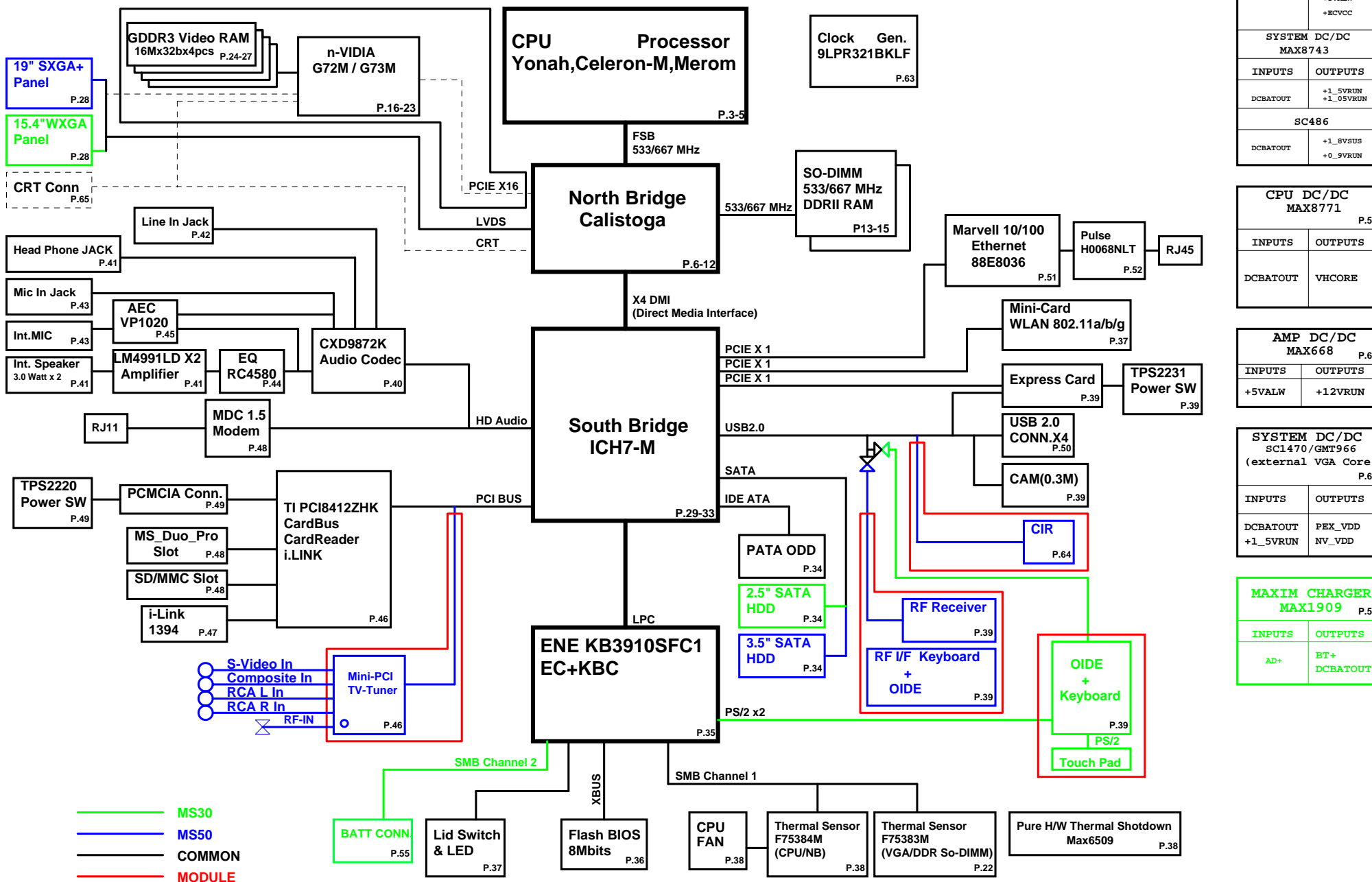
PCB P/N: - - - SA
 - - - SA
 - - - SA

Project Code & Schematics Subject: MS31/51 Main Board

P. Leader	Check by	Design by

FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
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MBX-152(CALISTOGA PM/GM+Gfx Block Diagram



SYSTEM DC/DC MAX8734A P.56	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +BCVCC
SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN +1_05VRUN
SC486	
DCBATOUT	+1_8VSUS +0_9VRUN

CPU DC/DC MAX8771 P.59	
INPUTS	OUTPUTS
DCBATOUT	VHORE

AMP DC/DC MAX668 P.60	
INPUTS	OUTPUTS
+5VALW	+12VRUN

SYSTEM DC/DC SCI470/GMT966 (external VGA Core) P.63	
INPUTS	OUTPUTS
DCBATOUT	PEX_VDD NV_VDD

MAXIM CHARGER MAX1909 P.54	
INPUTS	OUTPUTS
AD+	BT+ DCBATOUT

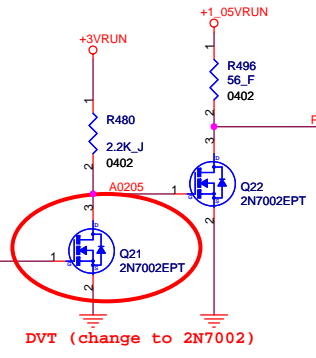
- MS30
- MS50
- COMMON
- MODULE

Layout note:
no stub on
H_STPCLK#

A#[32-39], APM#[0-1]:
Leave escape routing
on for future
functionality

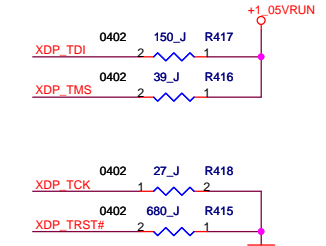
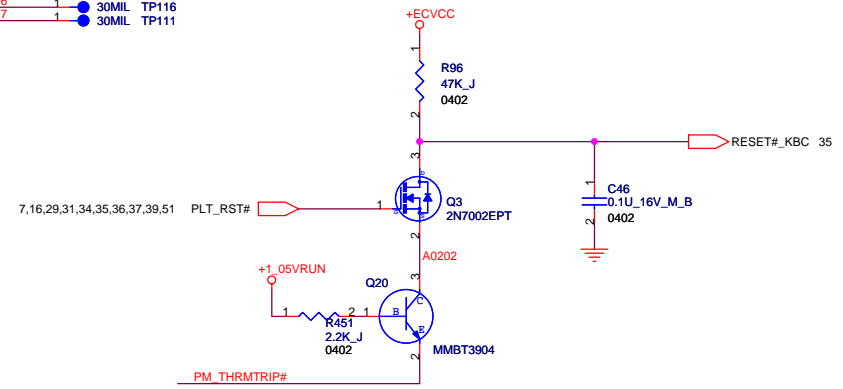
ICH7M's GPIO12: VIL----> -0.5V ~ 0.8V
VIH----> 2.0V ~ 3.3+0.5V
YONAH's PROCHOT#: VIL----> -0.1V ~ 0.3*VCCP
VIH----> 0.7*VCCP ~ VCCP+0.1

If PROCHOT# is routed between
CPU,IMVP and MCH, pull-up
resistor has to be 75 ohm +-5%

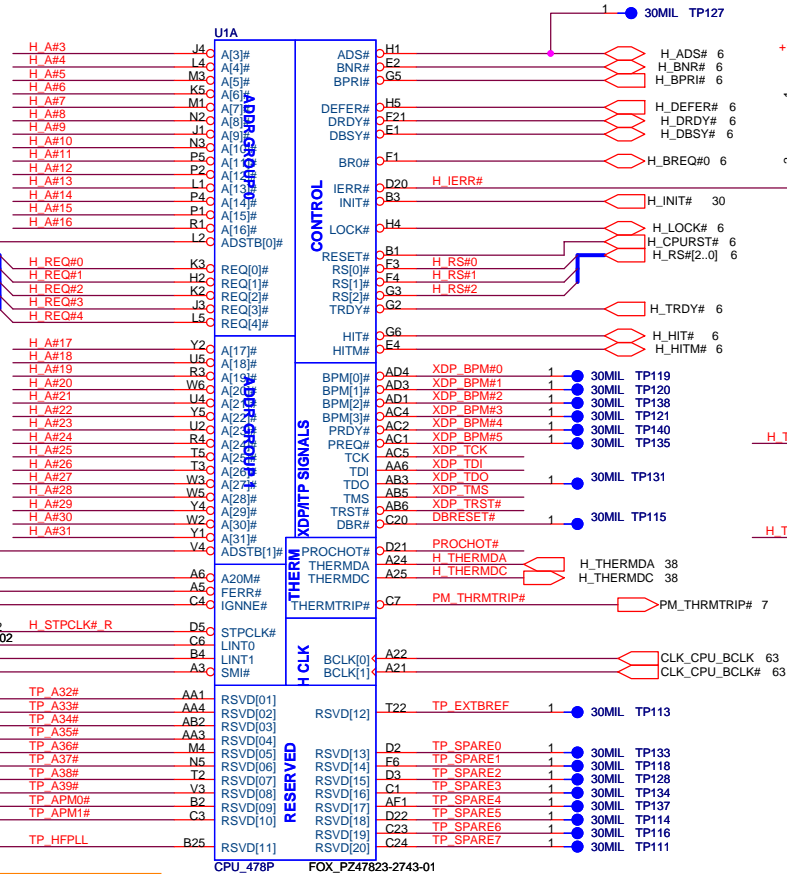


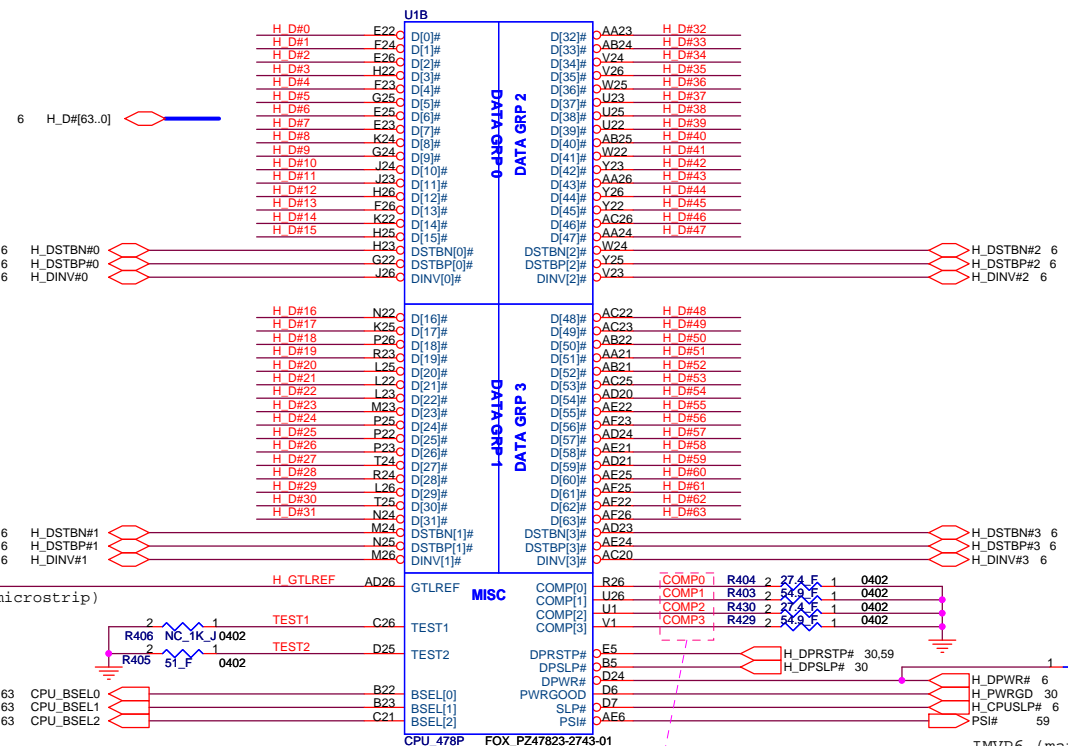
DVT (change to 2N7002)

TP139	30MIL	1	TP A32#	AA1	RSVD[01]	T22	TP EXTREF	1	30MIL	TP113
TP122	30MIL	1	TP A33#	AA4	RSVD[02]					
TP132	30MIL	1	TP A34#	AA2	RSVD[03]					
TP123	30MIL	1	TP A35#	AA3	RSVD[04]					
TP126	30MIL	1	TP A36#	M4	RSVD[05]	D2	TP SPARE0	1	30MIL	TP133
TP117	30MIL	1	TP A37#	N5	RSVD[06]	F6	TP SPARE1	1	30MIL	TP118
TP125	30MIL	1	TP A38#	T2	RSVD[07]	D3	TP SPARE2	1	30MIL	TP128
TP124	30MIL	1	TP A39#	V3	RSVD[08]	C1	TP SPARE3	1	30MIL	TP134
TP130	30MIL	1	TP APM0#	B2	RSVD[09]	AF1	TP SPARE4	1	30MIL	TP137
TP129	30MIL	1	TP APM1#	C3	RSVD[10]	D22	TP SPARE5	1	30MIL	TP114
					RSVD[11]	C23	TP SPARE6	1	30MIL	TP116
					RSVD[12]	C24	TP SPARE7	1	30MIL	TP111
					RSVD[20]					



Debug port not used .
resistors close to CPU.





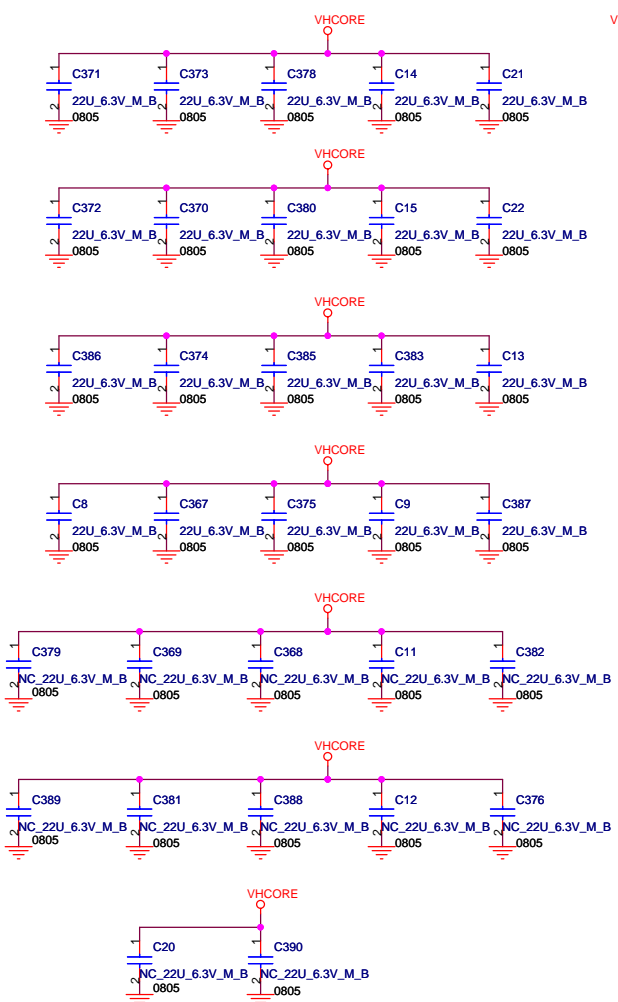
Place close to CPU
 Layout Note:
 Zo=55 ohm, 0.5"
 max for GTLREF.

FSB Frequency Table:

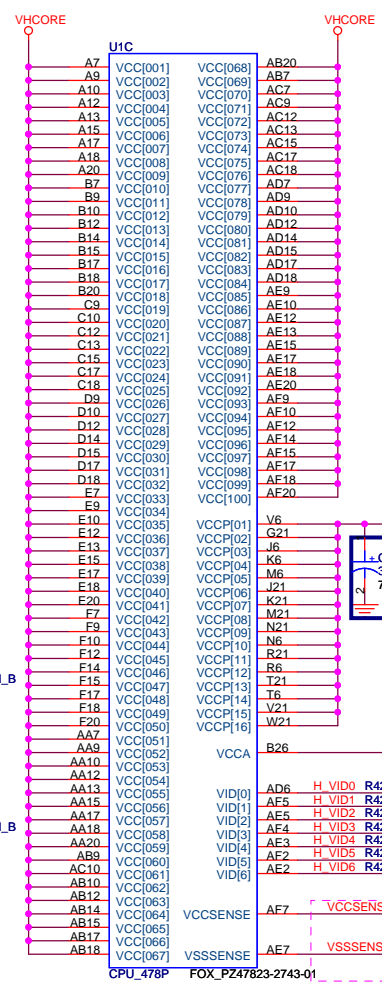
BSEL[2:0]	Freq.(MHz)
LLL	Reserve
LLH	133
LHL	Reserve
LHH	166

Layout Note:
 Comp0,2 connect with Zo=27.4 ohm, make trace length shorter then 0.5".
 Comp1,3 connect with Zo=55 ohm, make trace length shorter then 0.5".

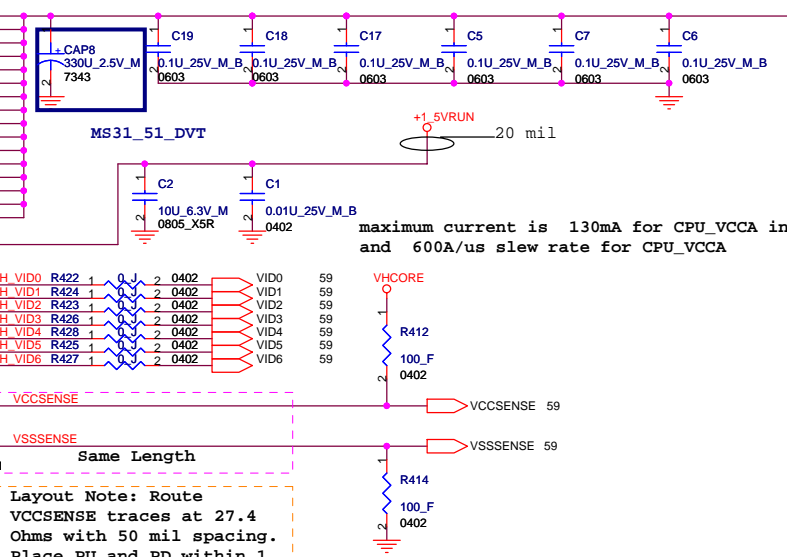
IMVP6 (max8771)
 cpu PSI# <-> max8771 PSI#
 max8771: VIHmin=0.67V
 VILmax=0.33V
 (ref. max8771 datasheet)



CRB :
add 12 dummy caps
0825



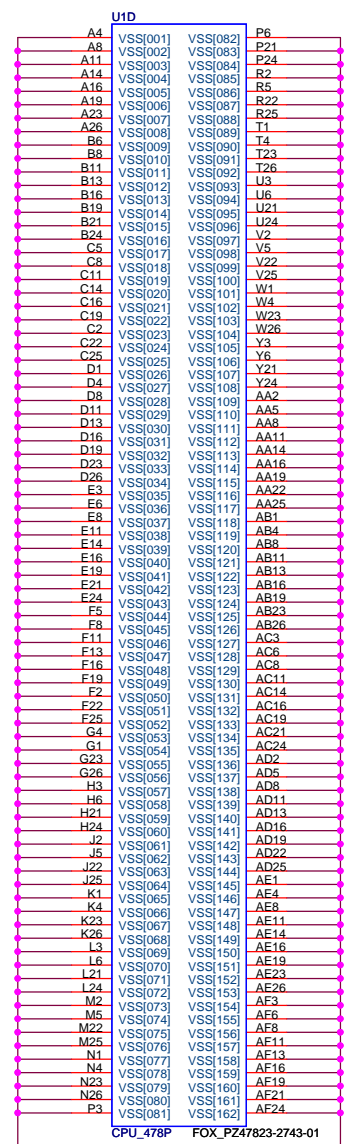
CPU_VCCA----->130mA
CPU_VCCP----->2.5A
CPU_VCC----->36A

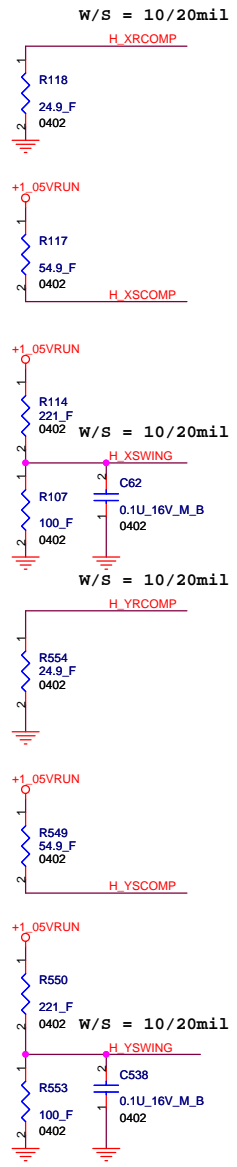


maximum current is 130mA for CPU_VCCA in Merom
and 600A/us slew rate for CPU_VCCA

Layout Note: Route
VCCSENSE traces at 27.4
Ohms with 50 mil spacing.
Place PU and PD within 1
inch of cpu.

width=18 mil
spacing=7 mil



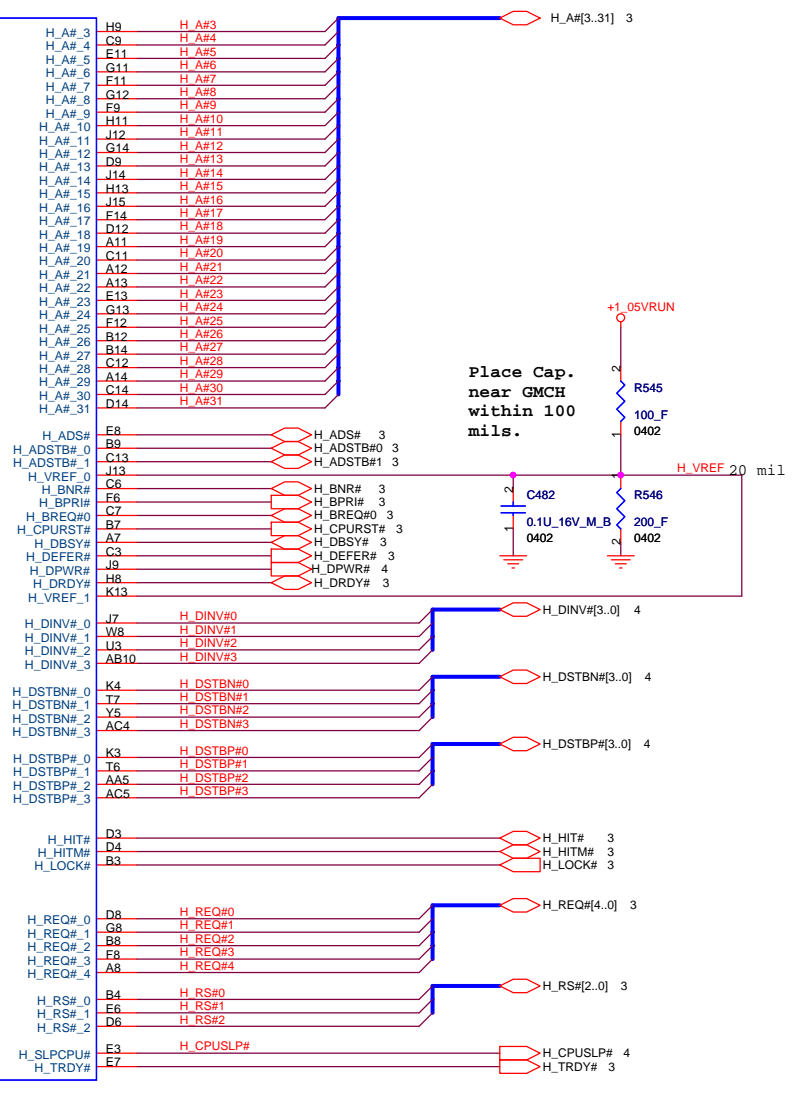


4 H_D#[63..0] H_D#[63..0]

U6A

H_D#0	F1	H_D#_0
H_D#1	J1	H_D#_1
H_D#2	H1	H_D#_2
H_D#3	J6	H_D#_3
H_D#4	H3	H_D#_4
H_D#5	K2	H_D#_5
H_D#6	G1	H_D#_6
H_D#7	G2	H_D#_7
H_D#8	K9	H_D#_8
H_D#9	K1	H_D#_9
H_D#10	K7	H_D#_10
H_D#11	J8	H_D#_11
H_D#12	H4	H_D#_12
H_D#13	J3	H_D#_13
H_D#14	K11	H_D#_14
H_D#15	G4	H_D#_15
H_D#16	T10	H_D#_16
H_D#17	W11	H_D#_17
H_D#18	T3	H_D#_18
H_D#19	U7	H_D#_19
H_D#20	U9	H_D#_20
H_D#21	U11	H_D#_21
H_D#22	T11	H_D#_22
H_D#23	W9	H_D#_23
H_D#24	T1	H_D#_24
H_D#25	T8	H_D#_25
H_D#26	T4	H_D#_26
H_D#27	W7	H_D#_27
H_D#28	U5	H_D#_28
H_D#29	T9	H_D#_29
H_D#30	W6	H_D#_30
H_D#31	T5	H_D#_31
H_D#32	AB7	H_D#_32
H_D#33	AA9	H_D#_33
H_D#34	W4	H_D#_34
H_D#35	W3	H_D#_35
H_D#36	Y3	H_D#_36
H_D#37	Y7	H_D#_37
H_D#38	W5	H_D#_38
H_D#39	Y10	H_D#_39
H_D#40	AB8	H_D#_40
H_D#41	W2	H_D#_41
H_D#42	AA4	H_D#_42
H_D#43	AA7	H_D#_43
H_D#44	AA2	H_D#_44
H_D#45	AA6	H_D#_45
H_D#46	AA10	H_D#_46
H_D#47	Y8	H_D#_47
H_D#48	AA1	H_D#_48
H_D#49	AB4	H_D#_49
H_D#50	AC9	H_D#_50
H_D#51	AB11	H_D#_51
H_D#52	AC11	H_D#_52
H_D#53	AB3	H_D#_53
H_D#54	AC2	H_D#_54
H_D#55	AD1	H_D#_55
H_D#56	AD9	H_D#_56
H_D#57	AC1	H_D#_57
H_D#58	AD7	H_D#_58
H_D#59	AC6	H_D#_59
H_D#60	AB5	H_D#_60
H_D#61	AD10	H_D#_61
H_D#62	AD4	H_D#_62
H_D#63	AC8	H_D#_63

HOST



Place Cap.
near GMCH
within 100
mils.

63 CLK_MCH_BCLK#
63 CLK_MCH_BCLK#

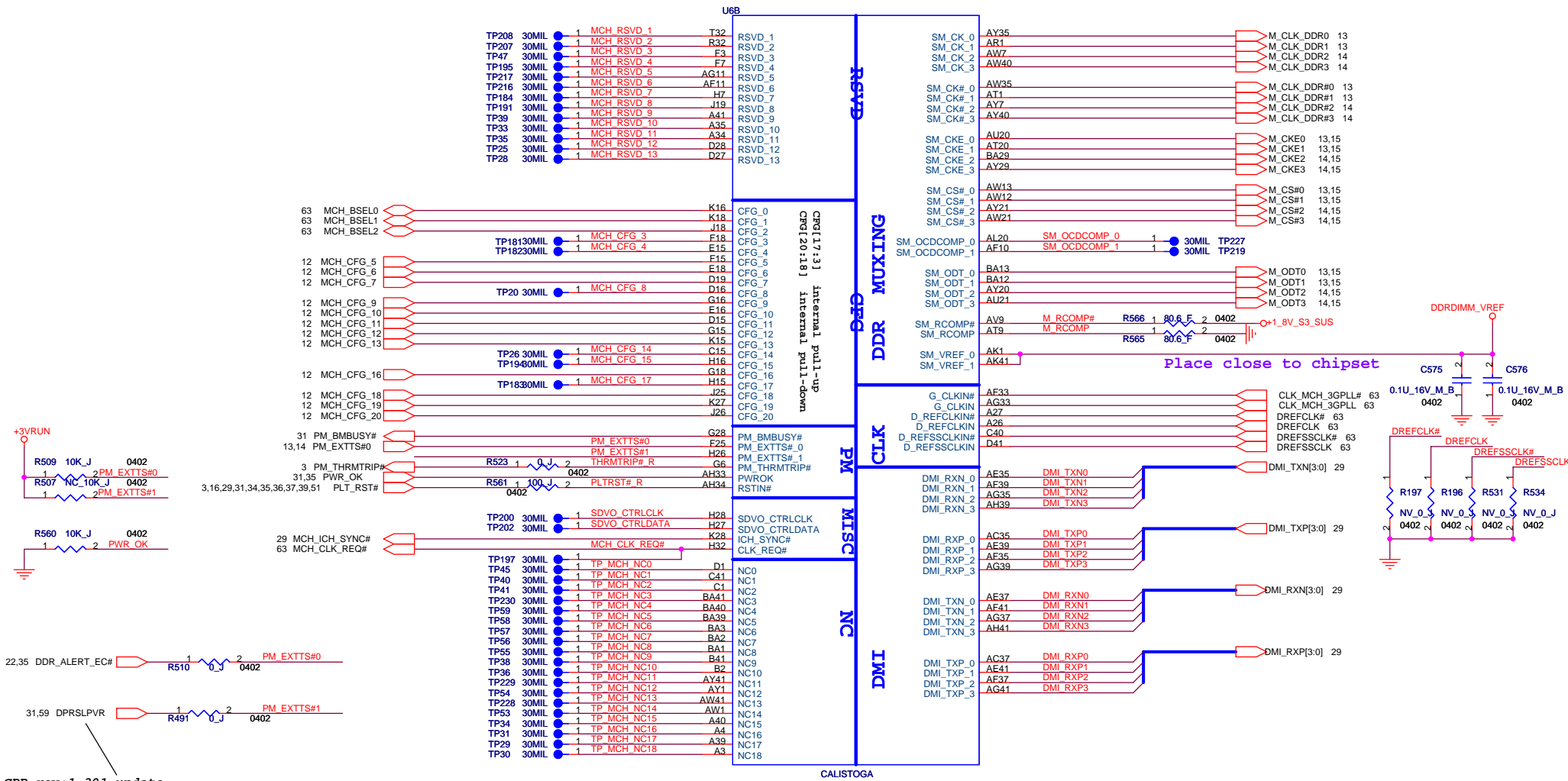
GM QG88CGM 12-0G88CGM-0000
PM QG88CPM 12-0G88CPM-0000
GM QG82945GM-A3 12-0G82945-A300 for MP

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Title **CALISTOHA (HOST)**

Size A3 Document Number **MS51(MBX-152)** Rev 0.30

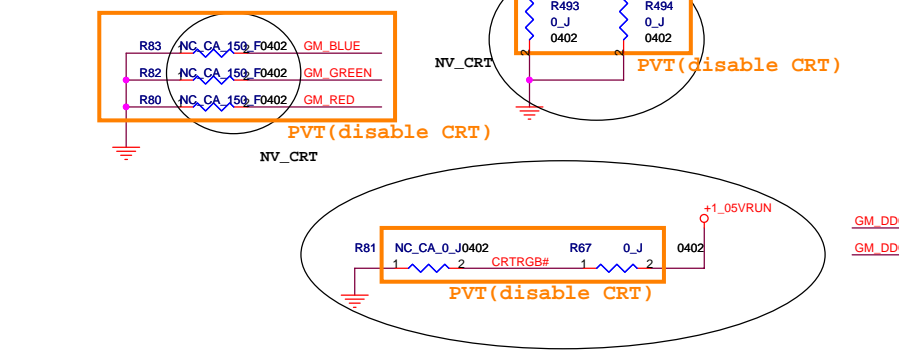
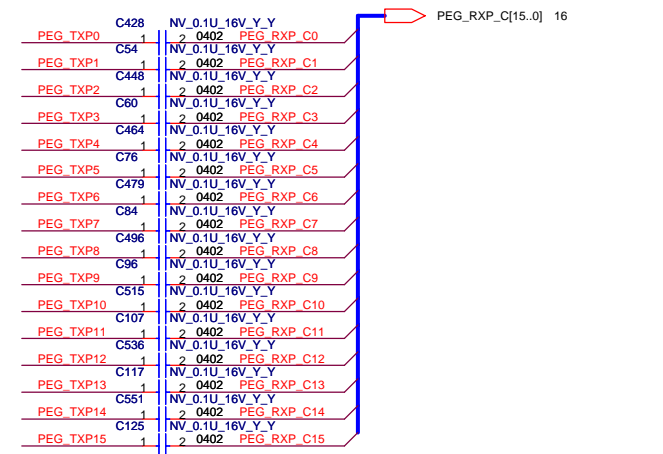
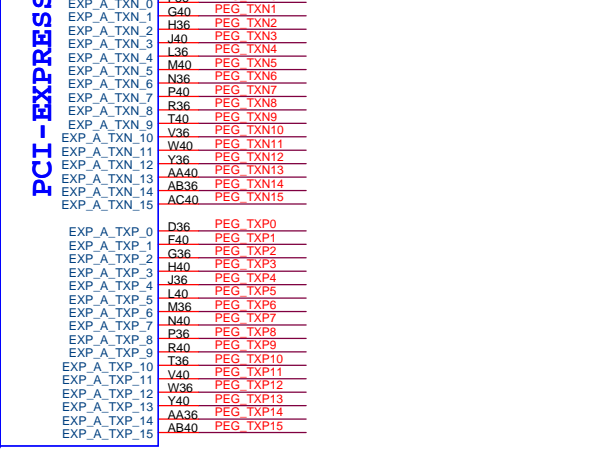
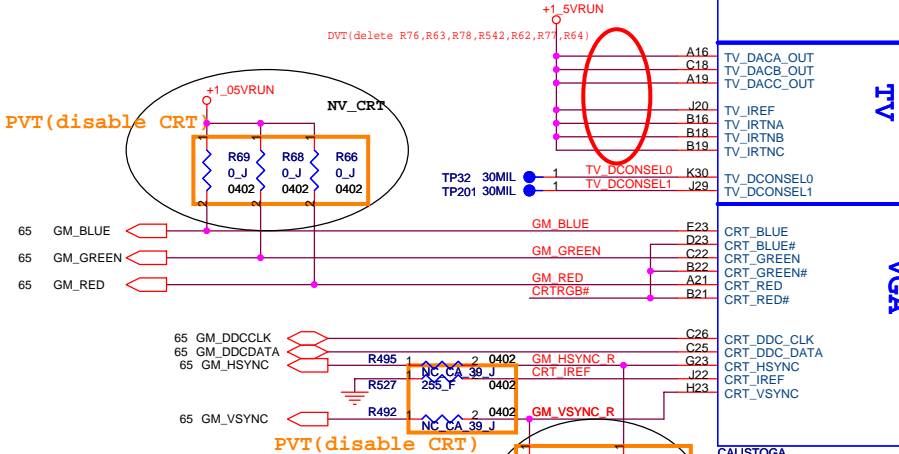
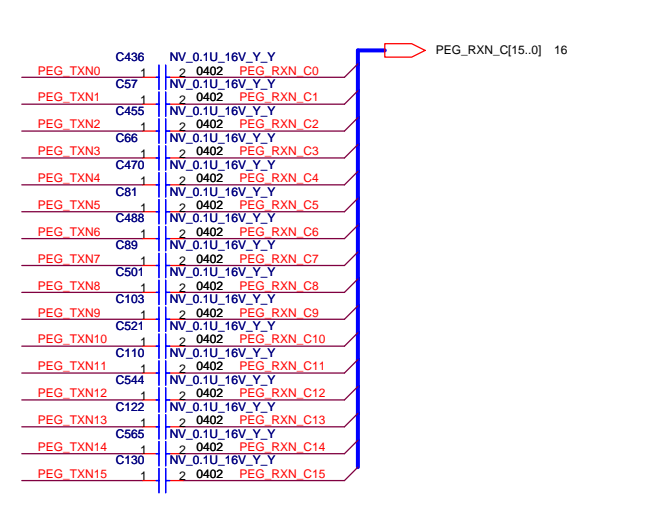
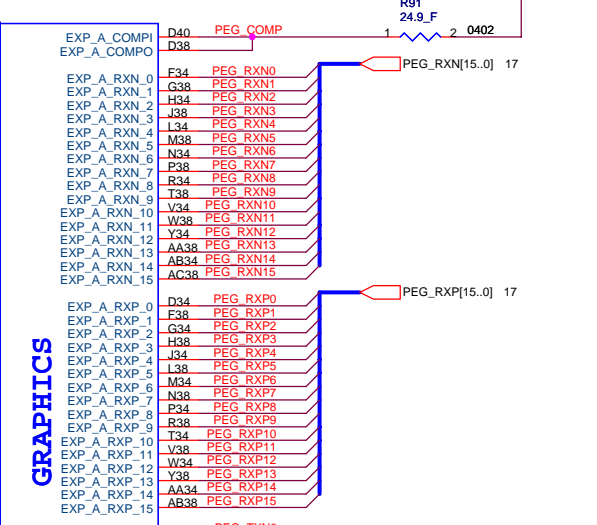
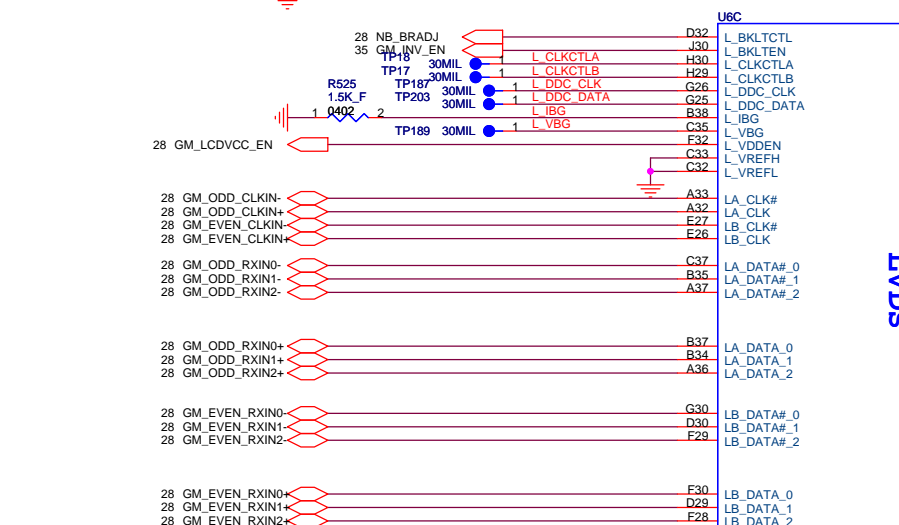
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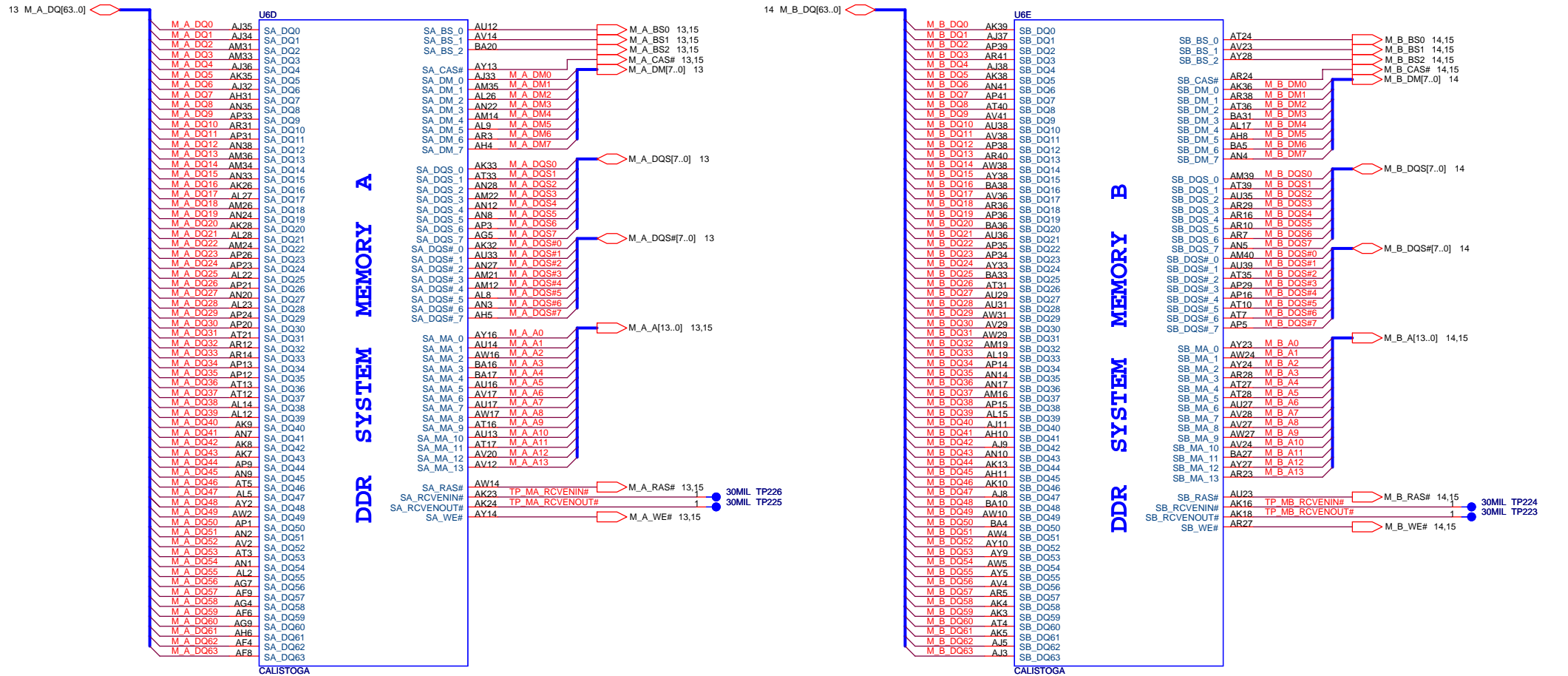


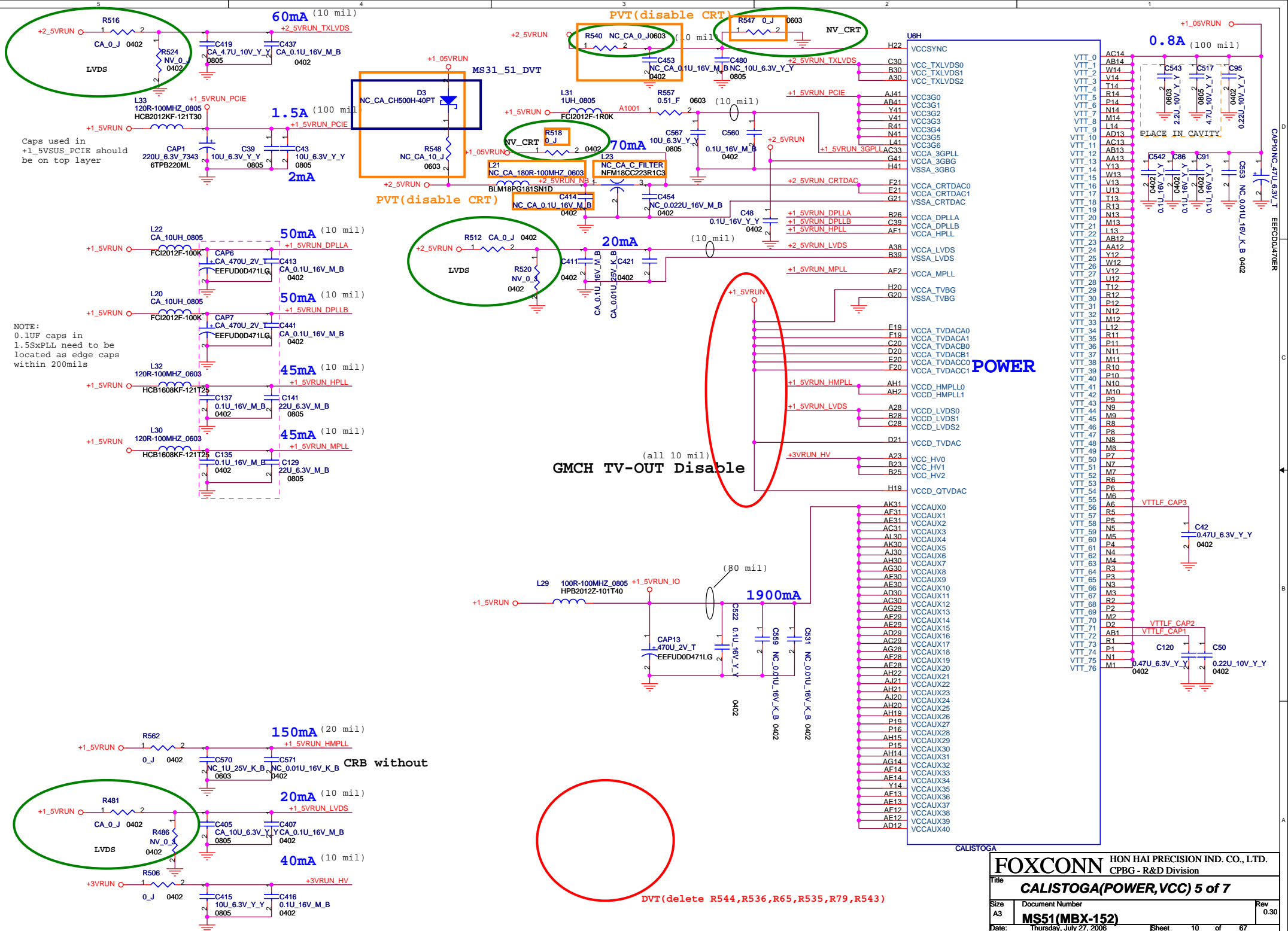
CRB rev:1.301 update

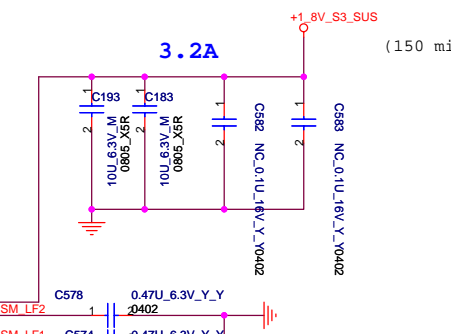
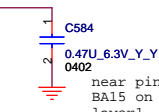
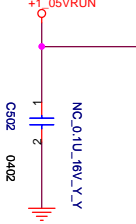
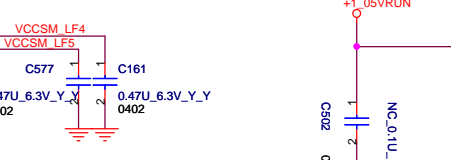
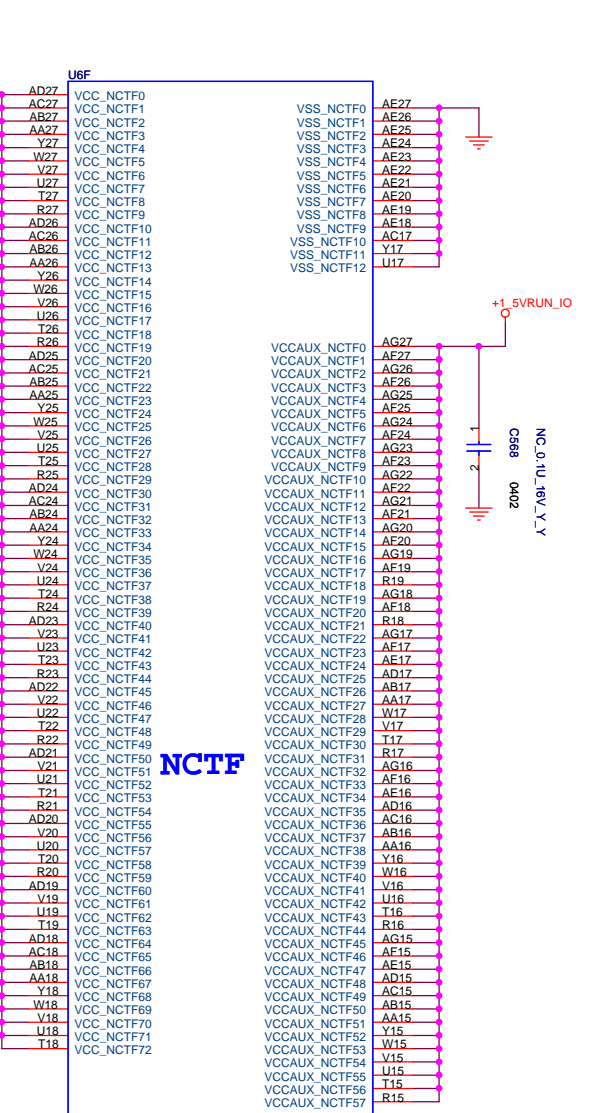
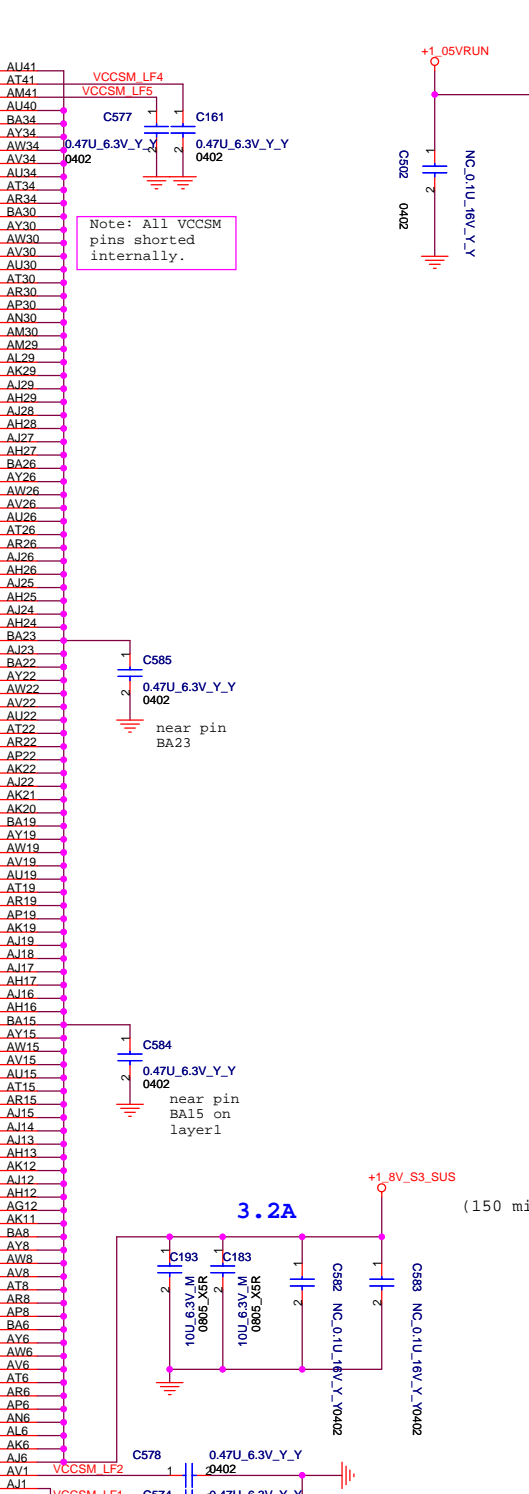
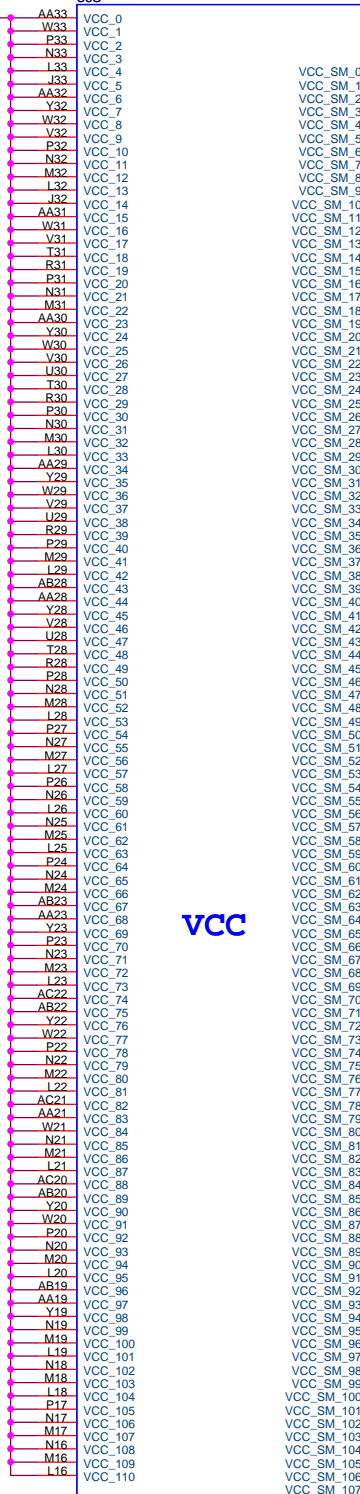
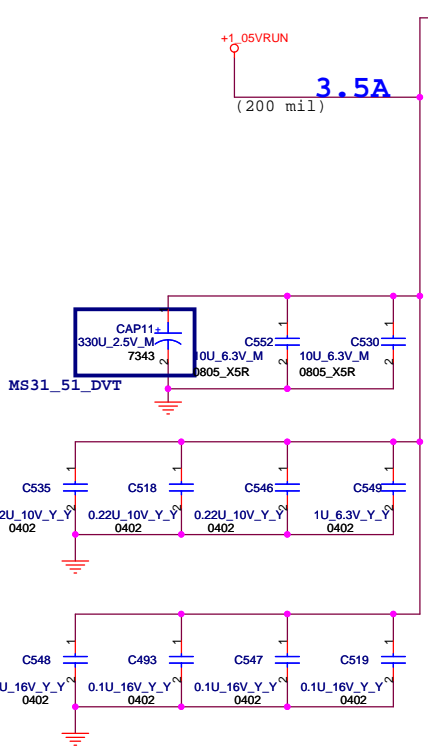
GM_INV_EN R539 1 100K J 2 0402

+1.5VRUN_PCIE









CALISTOGA

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 CPBG - R&D Division

Title: **CALISTOGA(VCC CORE) 6 of 7**

Size	Document Number	Rev
Custom	MS51(MBX-152)	0.30
Date:	Thursday, July 27, 2006	Sheet 11 of 67

7 MCH_CFG_5 ← 1 ● 30MIL TP193

MCH_CFG_5
Low = DMIX2
High = DMIX4

7 MCH_CFG_6 ← 1 ● 30MIL TP180

MCH_CFG_6
Low = Moby Dick
High = Calistoga
DDR2 select (default high)

7 MCH_CFG_7 ← 1 ● 30MIL TP15

MCH_CFG_7 (CPU Strap)
Low = RSVD
High = Mobile Yonah processor

7 MCH_CFG_9 ← 1 ● 30MIL TP250

MCH_CFG_9 (PCIe Graphics Lane)
Low = Reverse Lane operation
High = Normal operation

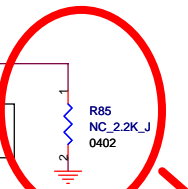
For layout convenience

7 MCH_CFG_10 ← 1 ● 30MIL TP192

MCH_CFG_10 (HOST PLL VCC SELECT)
Low = RESERVED
High = MOBILITY

7 MCH_CFG_11 ← 1 ● 30MIL TP185

MCH_CFG_11 (PSB 4x CLK ENABLE)
Low = Reserved
High = Calistoga



Layout Noe:
Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub

7 MCH_CFG_12 ← 1 ● 30MIL TP185

7 MCH_CFG_13 ← 1 ● 30MIL TP205

MCH_CFG_[13:12] (XOR/ALLZ)
00=Partial Clock Gating Disable
01=XOR Mode Enable
10=All-Z Mode Enable
11=Normal Operation(Default)

7 MCH_CFG_16 ← 1 ● 30MIL TP178

MCH_CFG_16 (FSB Dynamic ODT)
Low = Dynamic ODT Disabled
High = Dynamic ODT Enable

MCH_CFG_18 (VCC_CORE Select)
Low = 1.05V(default)
High = 1.5V

7 MCH_CFG_18 ← 1 ● 30MIL TP248

DVT (delete R508,add TP)

MCH_CFG_19 (DMI LANE REVERSAL)
Low = Normal(default)
High = LANES REVERSED

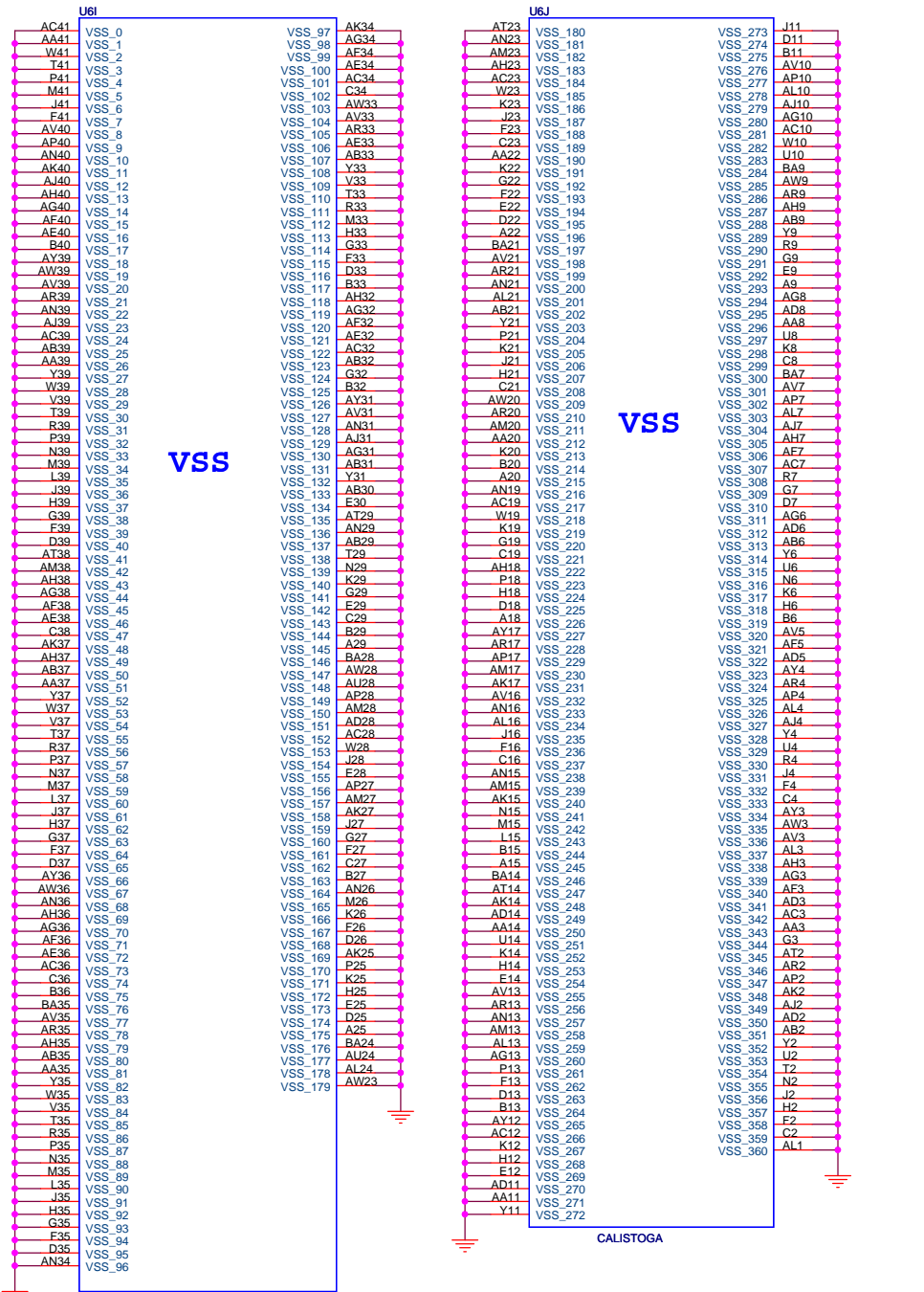
7 MCH_CFG_19 ← 1 ● 30MIL TP249

DVT (delete R541,add TP)

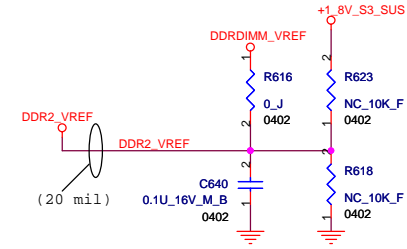
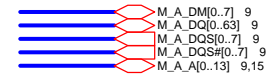
MCH_CFG_20 (PCIe Backward Interoperability mode)
Low = Only SDVO or PCIE x1 is operational (defaults)
High = SDVO and PCIE x1 are operating simultaneously via the PEG port

7 MCH_CFG_20 ← 1 ● 30MIL TP204

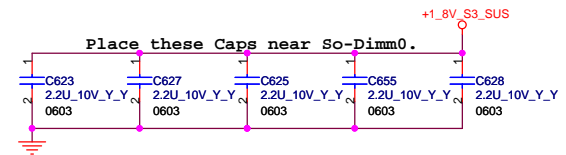
Check CALISTOGA version , after A2 version , if systec can't boot up then NC the pull low R



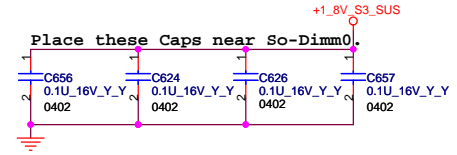
1.8V per DIMM=3.08A



Close to DIMM

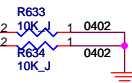


Place these Caps near So-Dimm0.

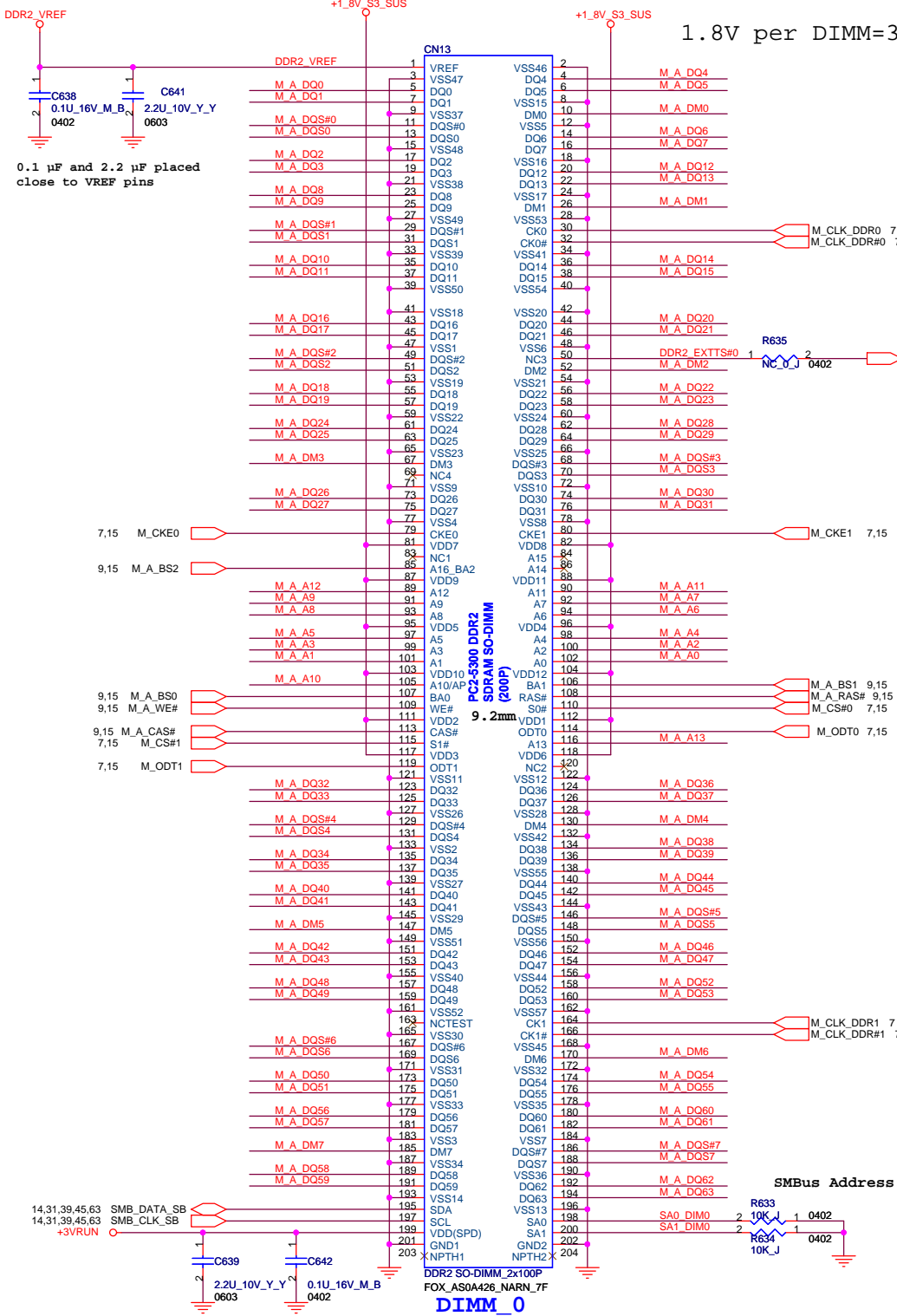


Place these Caps near So-Dimm0.

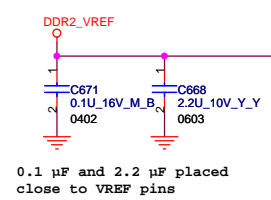
SMBus Address: A0(W)/A1(R)



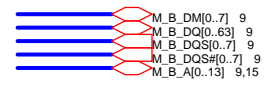
FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title DDR(I)SO-DIMM_0		
Size A3	Document Number MS51(MBX-152)	Rev 0.30
Date: Thursday, July 27, 2006	Sheet 13	of 67



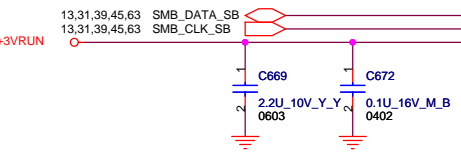
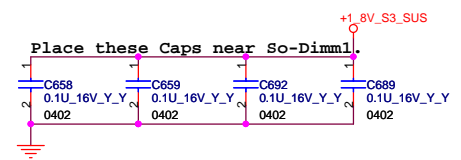
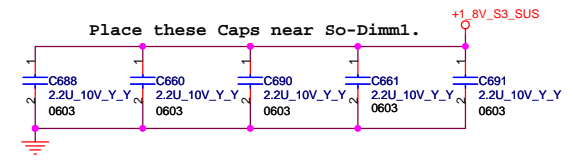
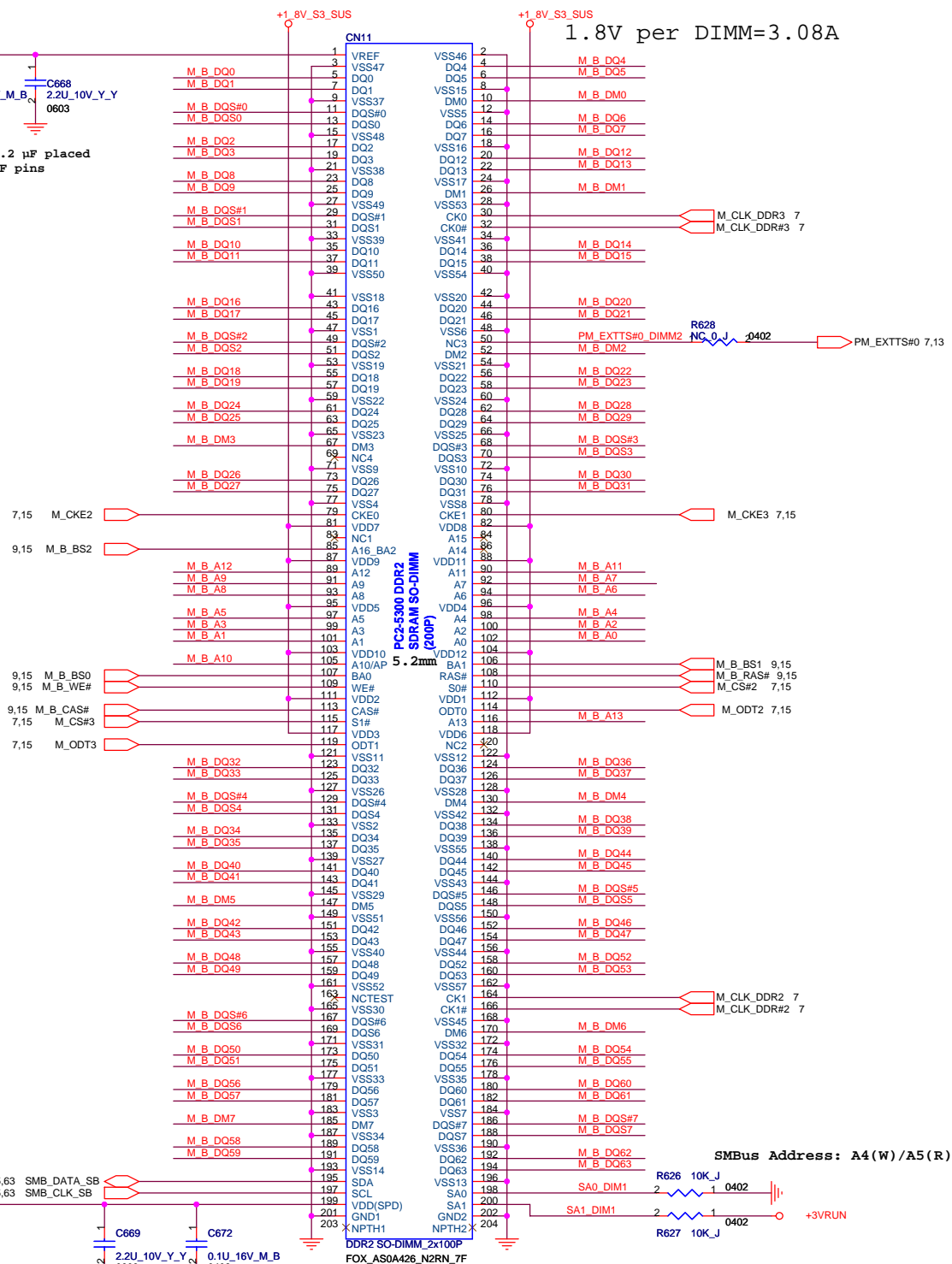
DIMM_0



1.8V per DIMM=3.08A

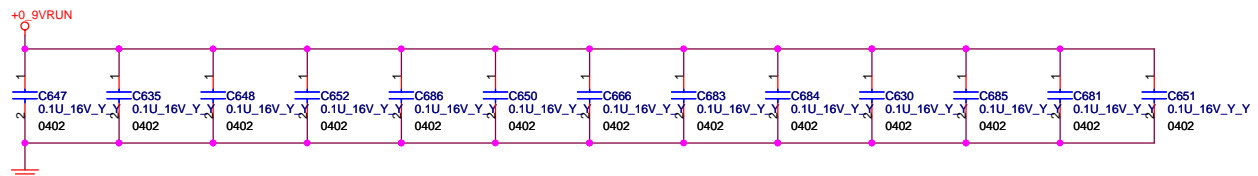


0.1 uF and 2.2 uF placed close to VREF pins

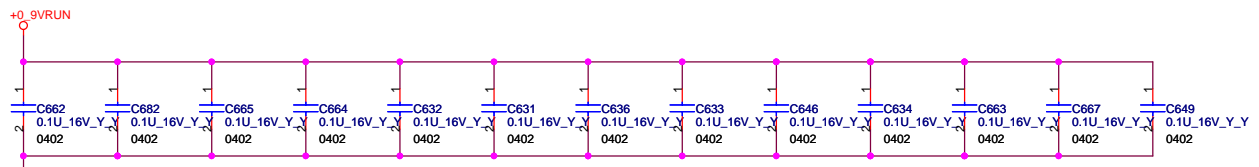


DIMM_1

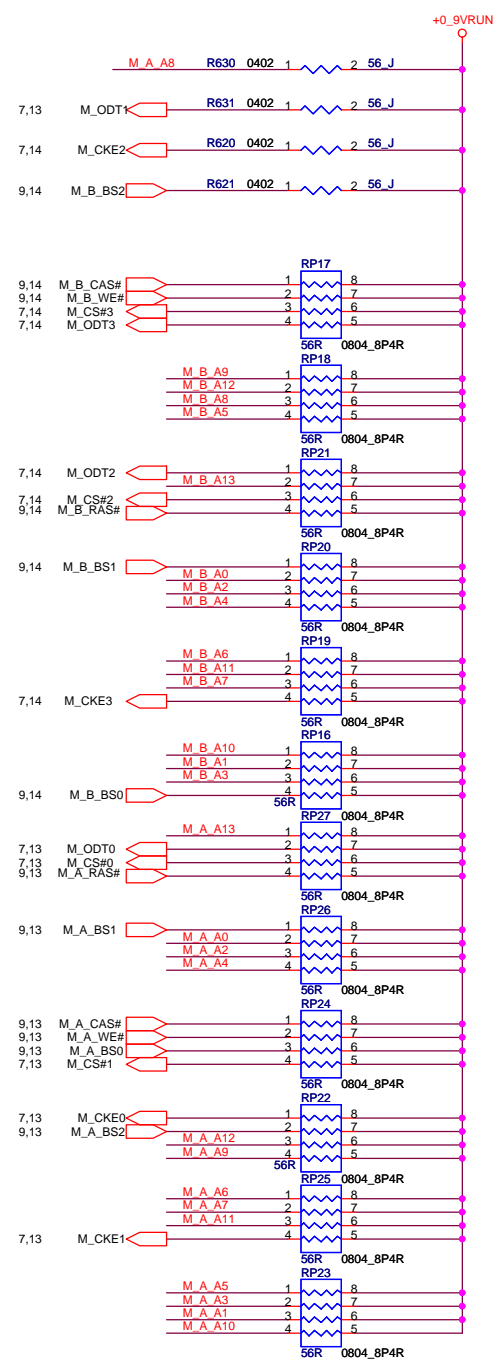
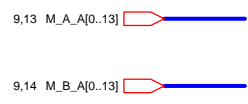
FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title DDR(II)SO-DIMM_1			
Size A3	Document Number		Rev 0.30
MS51(MBX-152)			
Date: Thursday, July 27, 2006	Sheet 14	of 67	

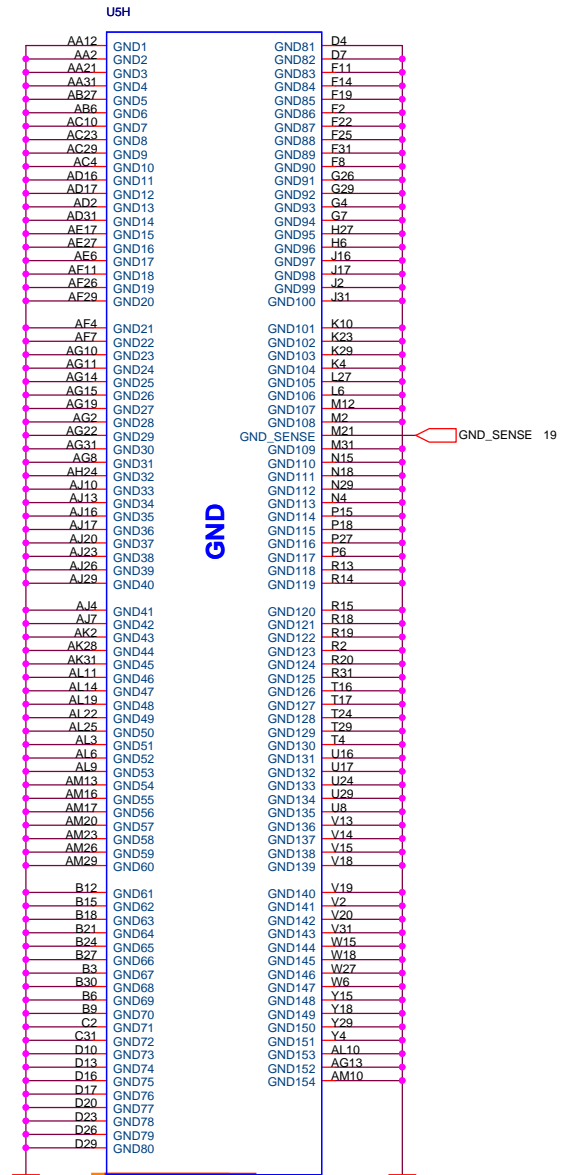
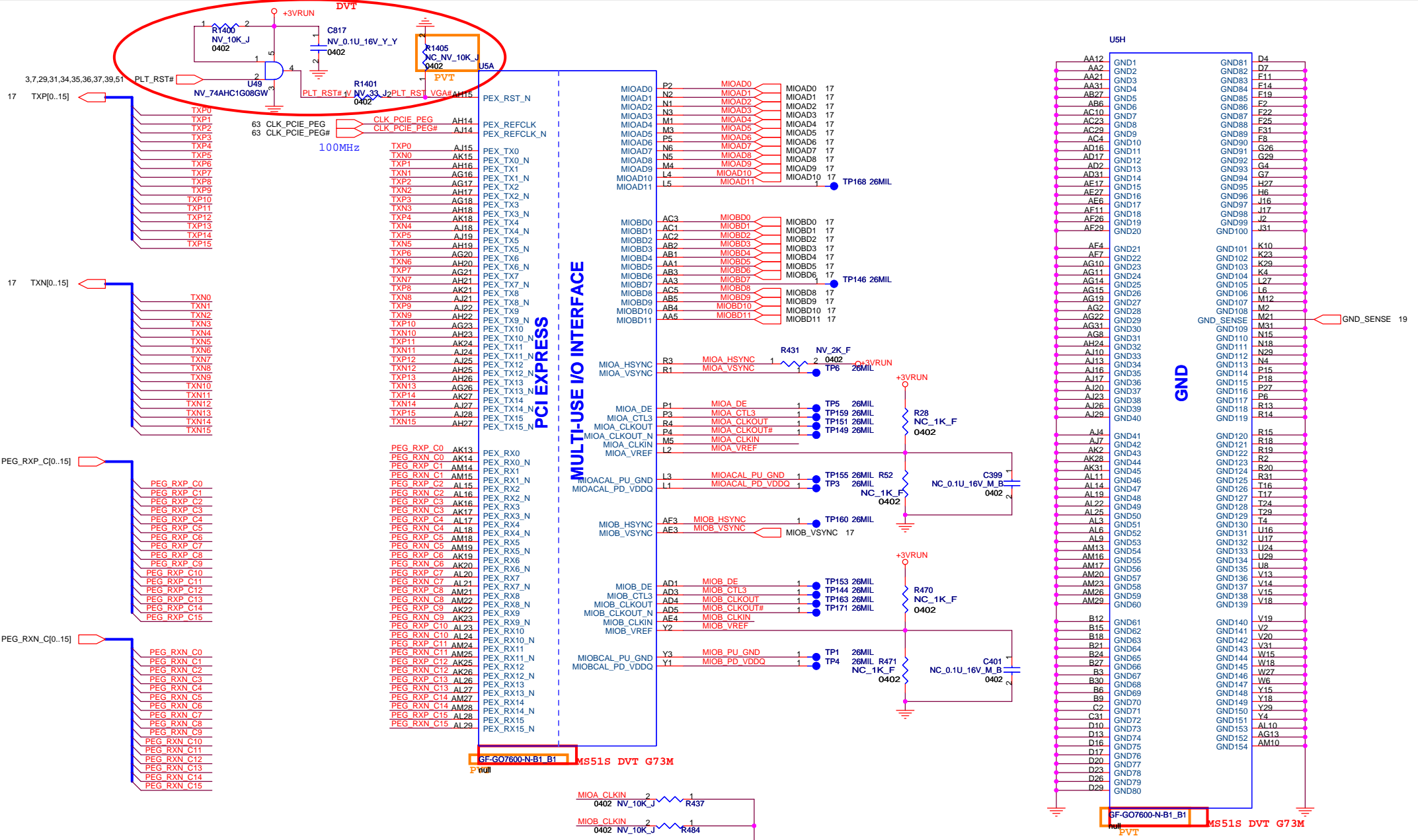


Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VRUN



Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VRUN





TVMODE		
NTSC (01)		
MIOAD10	MIOAD7	TVMODE
0	0	SECAM
0	1	NTSC
1	0	PAL
1	1	CRT

Strap for GDDR3-136ball

0001	16Mx32	Infineon
0010	16Mx32	Hynix
0011	16Mx32	Samsung
0101	8Mx32	Infineon
0110	8Mx32	Hynix
0111	8Mx32	Samsung

SUBVENDOR

0	(USE SYSTEM BIOS)
1	(USE EXTERNAL ROM)

PANEL ID CONFIG
NC

MIOAD0 is used to set the PCI Express PLL termination enable. DEFAULT "0"

3GIO_PADCFG[2:0]
001 for G7X
DVT change to 001

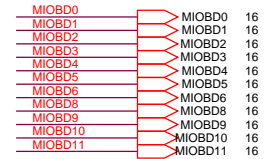
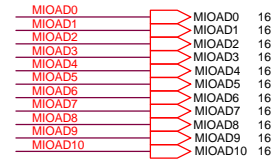
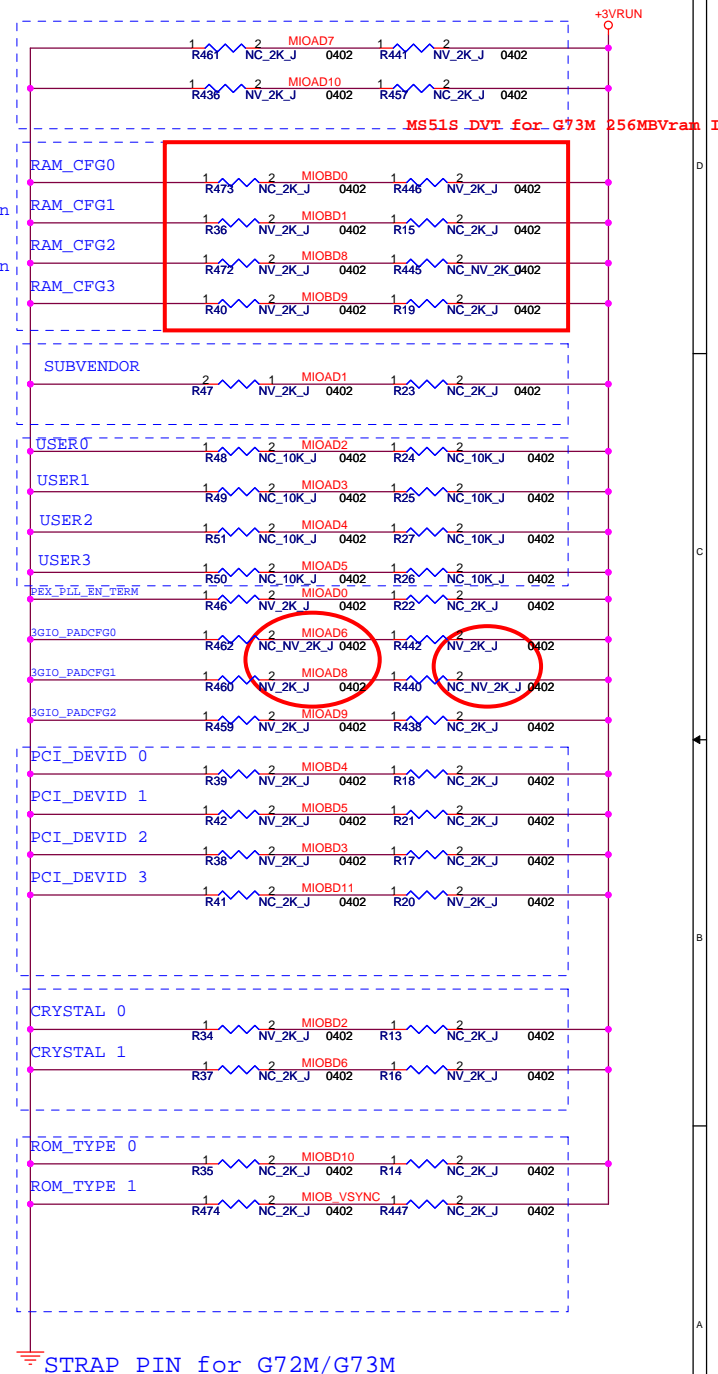
G72M/G73M
PCI_DEVID[3:0]="1000"-->8

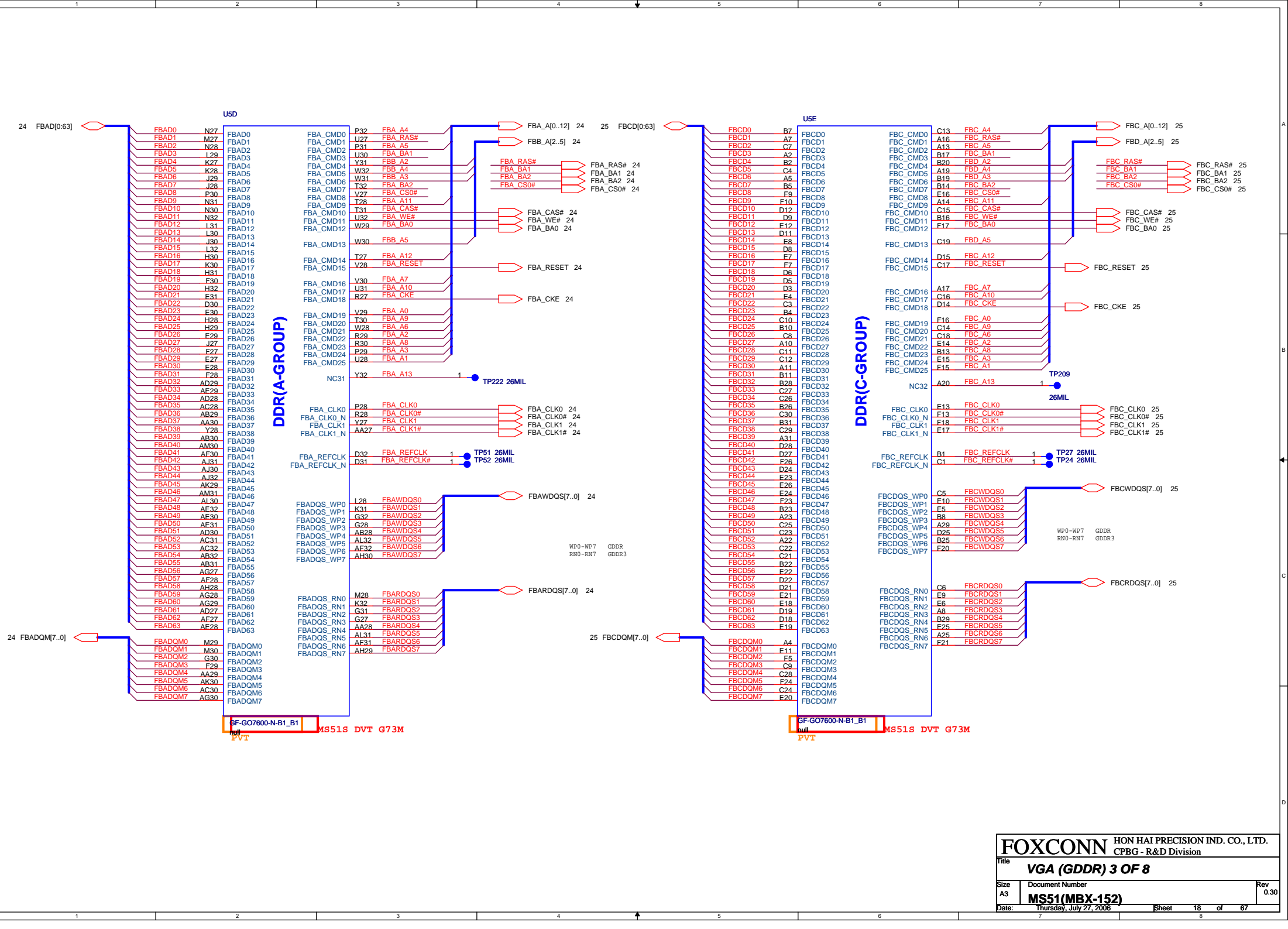
CRYSTAL
10 (27M Hz)

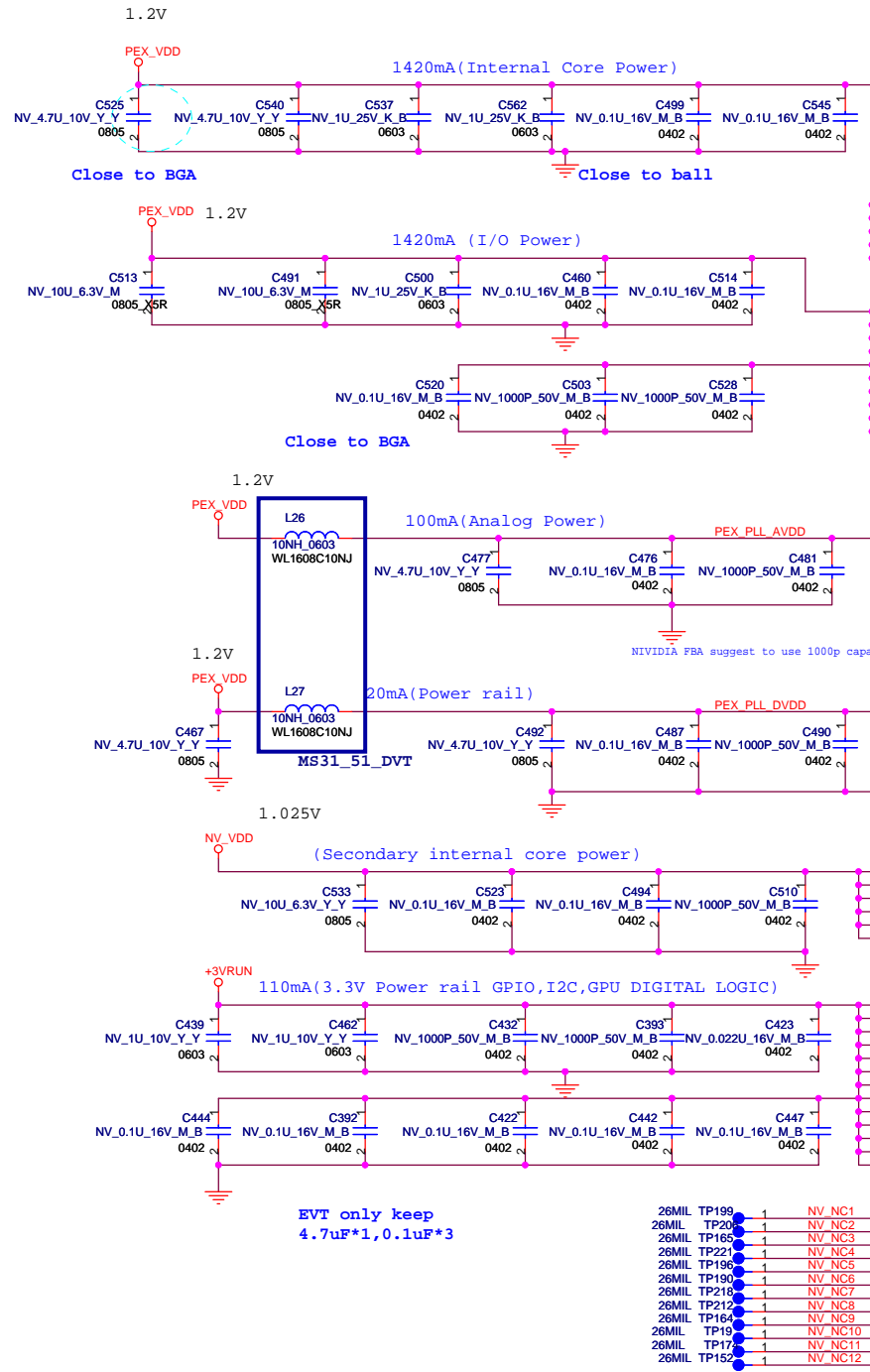
MIOBD6	MIOBD2	Crystal
1	0	27MHz
0	1	14.318MHz
0	0	13.5MHz
1	1	Preserved

ROM_TYPE NC

00	PARALLEL
01	SERIAL_AT25F
10	SERIAL_SST45VF
11	LPC

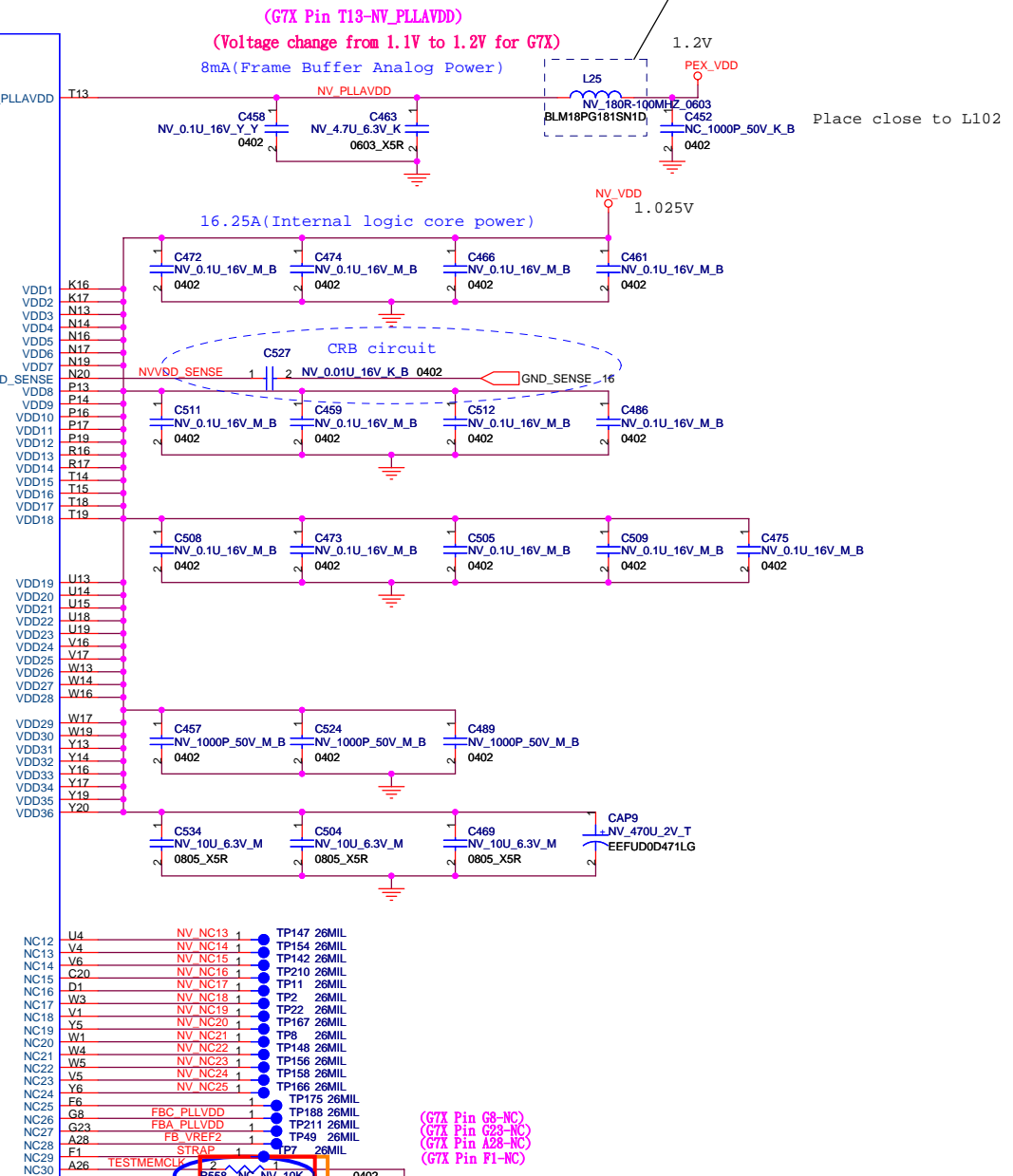






- USB
- AD23 PEX_IOVDD1
 - AF24 PEX_IOVDD2
 - AF23 PEX_IOVDD3
 - AE25 PEX_IOVDD4
 - AG24 PEX_IOVDD5
 - AG25 PEX_IOVDD6
- AC16 PEX_IOVDDQ1
- AC17 PEX_IOVDDQ2
- AC21 PEX_IOVDDQ3
- AC22 PEX_IOVDDQ4
- AE18 PEX_IOVDDQ5
- AE22 PEX_IOVDDQ6
- AE12 PEX_IOVDDQ7
- AF18 PEX_IOVDDQ8
- AF21 PEX_IOVDDQ9
- AF22 PEX_IOVDDQ10
- PEX_IOVDDQ11
- AF15 PEX_PLLA VDD
- PEX_PLLDVDD
- AE15 PEX_PLLDVDD
- AE16 PEX_PLLGND
- VDD_LP1
- VDD_LP2
- VDD_LP3
- VDD_LP4
- VDD_LP5
- VDD_LP6
- VDD33_1
- VDD33_2
- VDD33_3
- VDD33_4
- VDD33_5
- VDD33_6
- VDD33_7
- VDD33_8
- VDD33_9
- VDD33_10
- VDD33_11
- VDD33_12
- VDD33_13
- NC1
- NC2
- SPDIF
- NC3
- NC4
- NC5
- NC6
- NC7
- NC8
- NC9
- NC10
- NC11

POWER



GF-GO7600-N-B1_B1
bull
PVT MS51S DVT G73M

G73M Pin A26-NC
G72M Pin A26 need stuff R305 10K

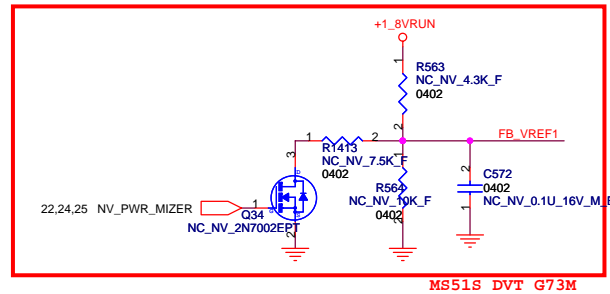
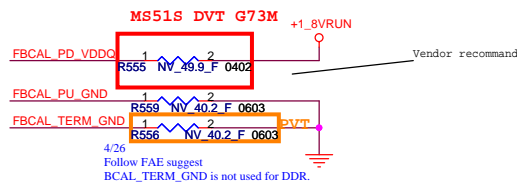
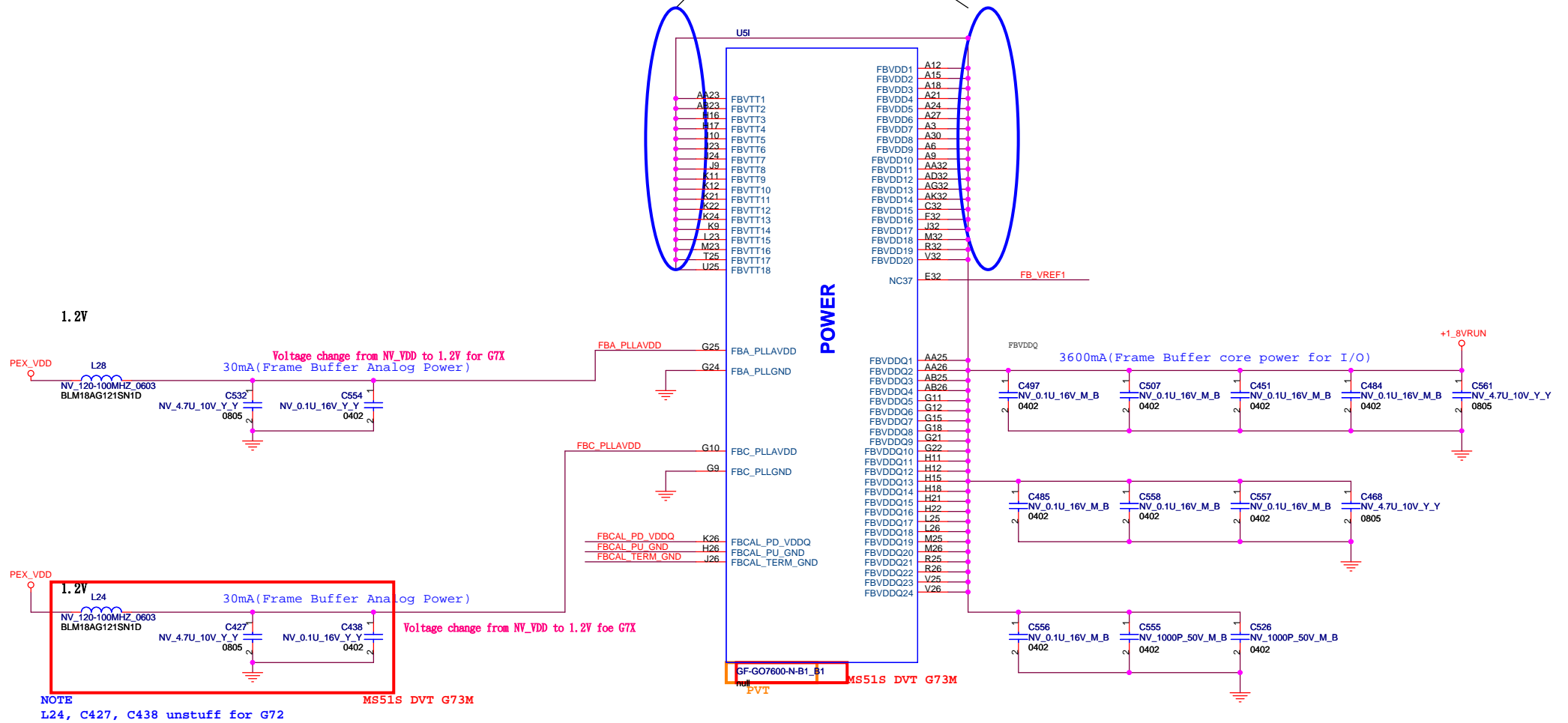
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

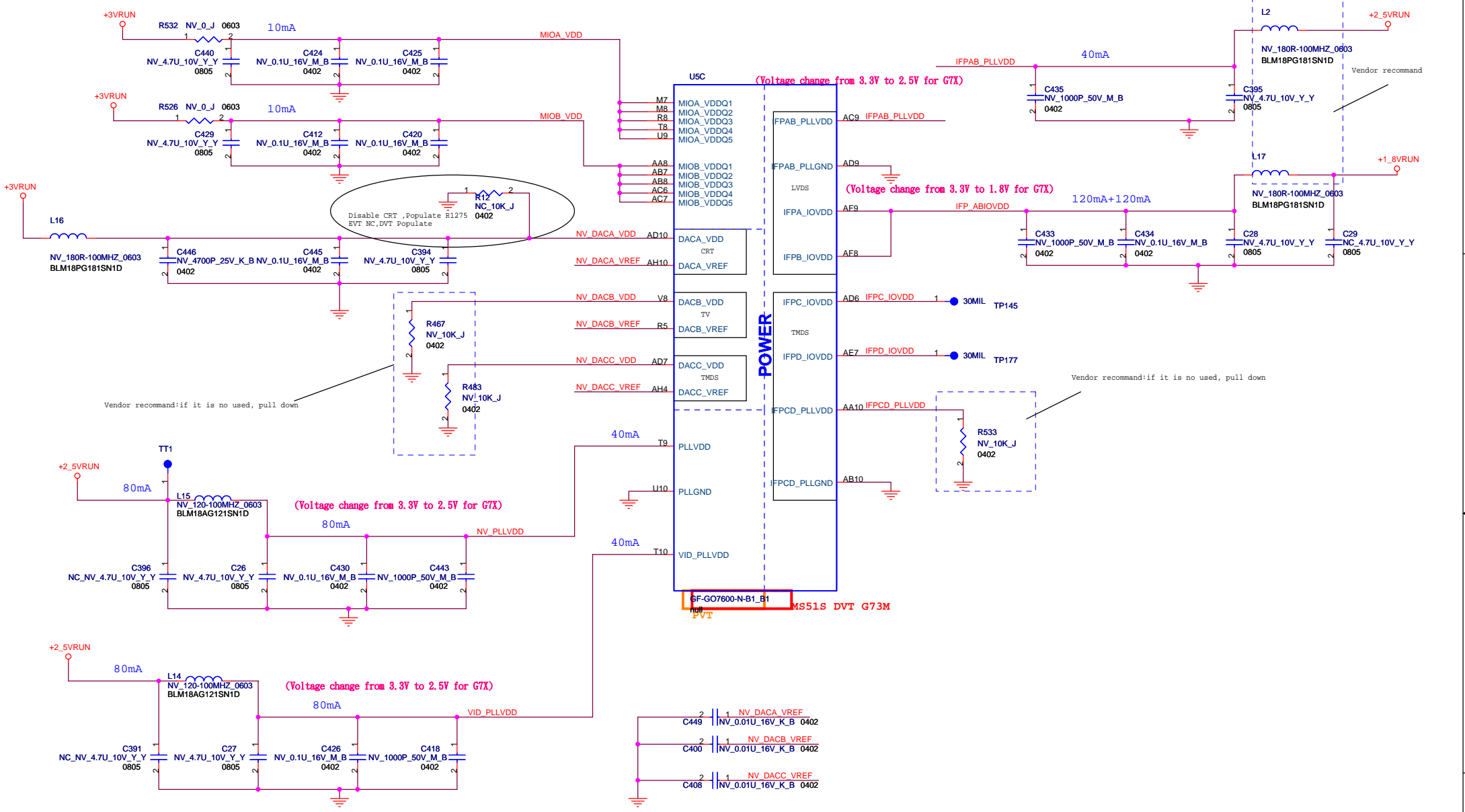
Title **VGA (POWER) 4 OF 8**

Size A3 Document Number **MS51(MBX-152)** Rev 0.30

Date: Thursday, July 27, 2006 Sheet 19 of 67

Follow FAE suggest the design guide table 4-4 and 4-5.
 DDR1 underminated solution,so FBVTT/FBVDQ/FBVDQ can connect together.
 for the power rails decoupling,FBVTT/FBVDQ do not require caps decoupling.
 only FVDDQ power rail required.





SM bus Address :
1001100(BC)
For F75383M

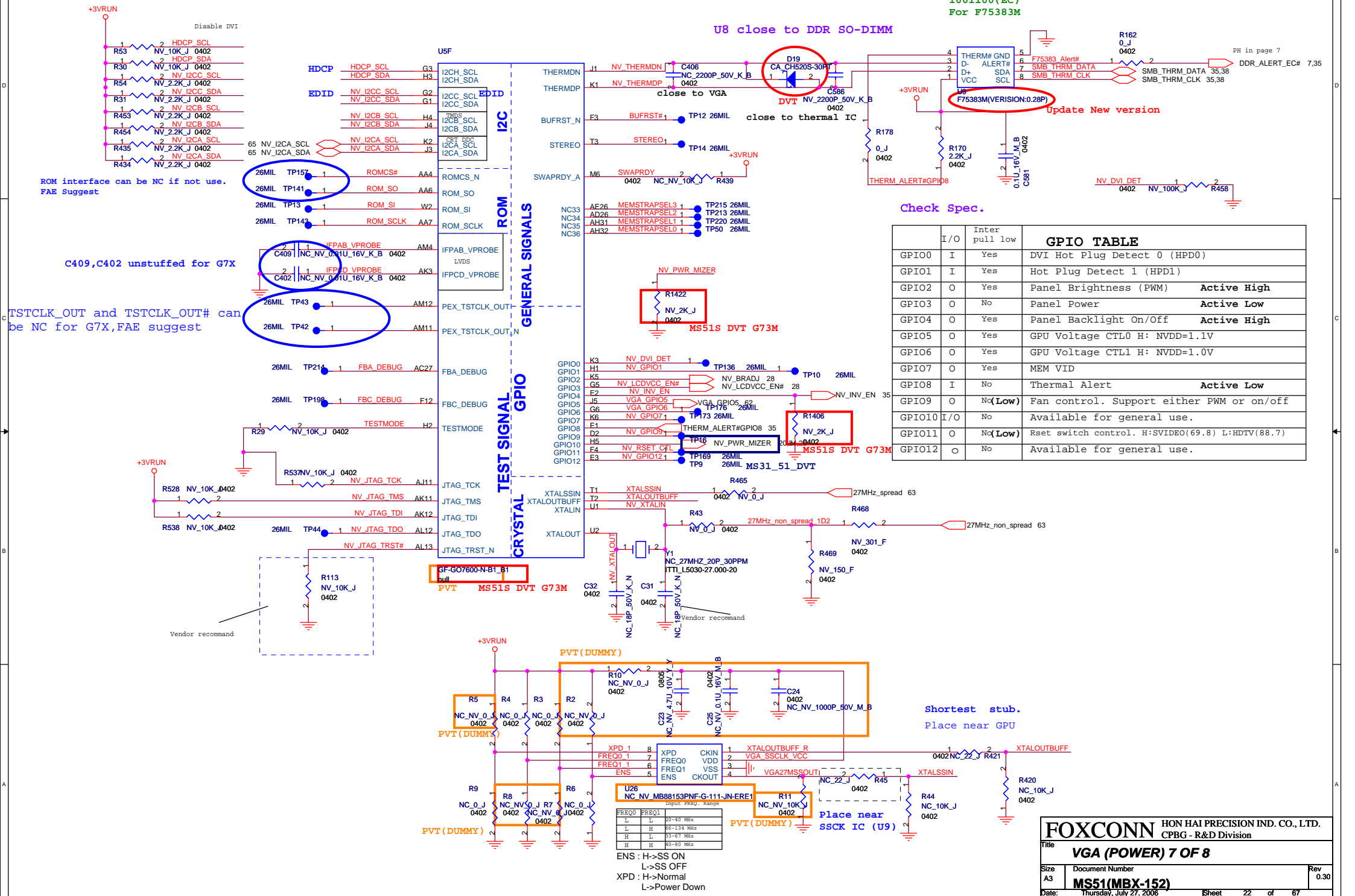
U8 close to DDR SO-DIMM

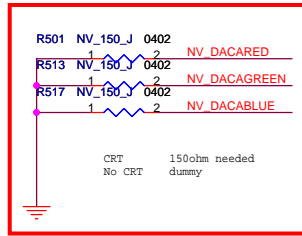
PH in page 7
DDR_ALERT_EC# 7,35

Update New version

Check Spec.

	I/O	Inter pull low	GPIO TABLE
GPIO0	I	Yes	DVI Hot Plug Detect 0 (HPD0)
GPIO1	I	Yes	Hot Plug Detect 1 (HPD1)
GPIO2	O	Yes	Panel Brightness (PWM) Active High
GPIO3	O	No	Panel Power Active Low
GPIO4	O	Yes	Panel Backlight On/Off Active High
GPIO5	O	Yes	GPU Voltage CTL0 H: NVDD=1.1V
GPIO6	O	Yes	GPU Voltage CTL1 H: NVDD=1.0V
GPIO7	O	Yes	MEM VID
GPIO8	I	No	Thermal Alert Active Low
GPIO9	O	No(Low)	Fan control. Support either PWM or on/off
GPIO10	I/O	No	Available for general use.
GPIO11	O	No(Low)	Rset switch control. H:SVIDEO(69.8) L:HDTV(88.7)
GPIO12	O	No	Available for general use.

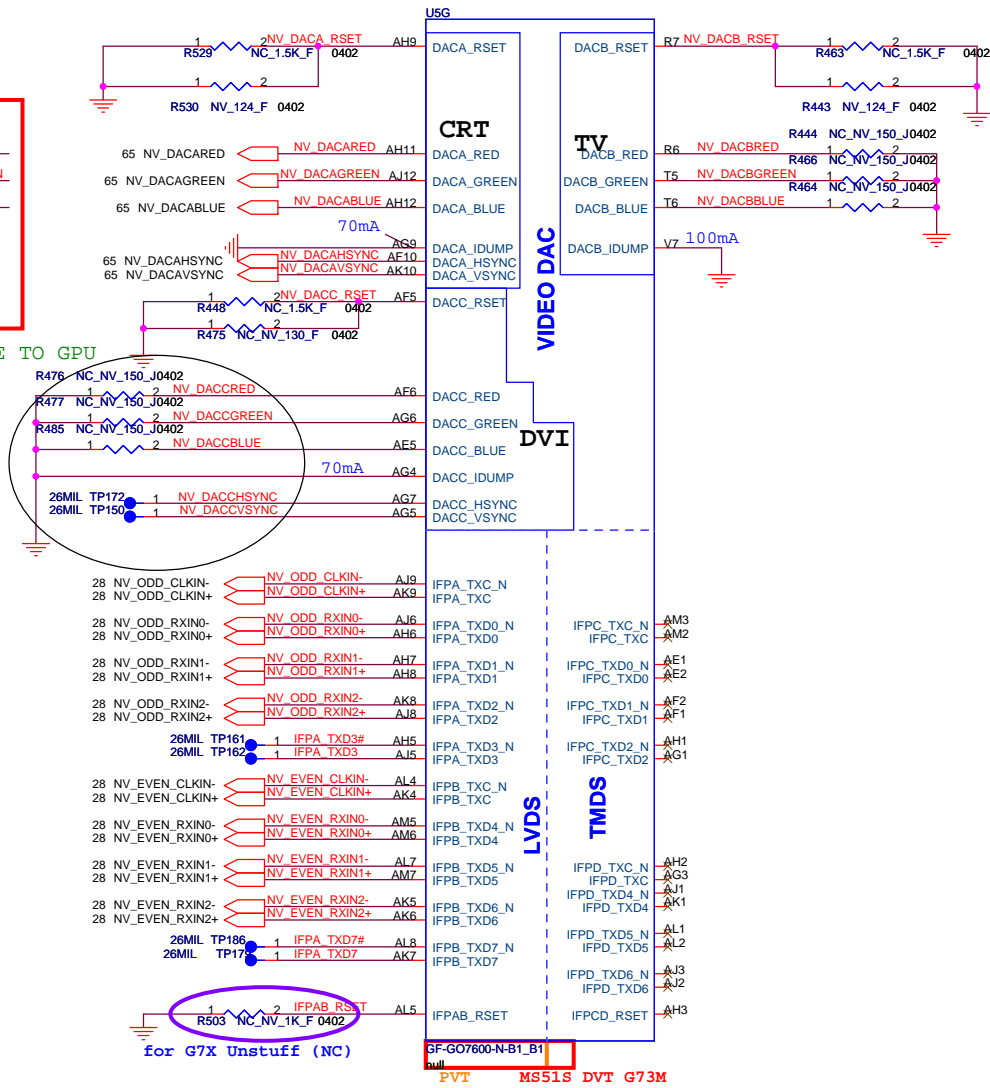




MS51S DVT G73M

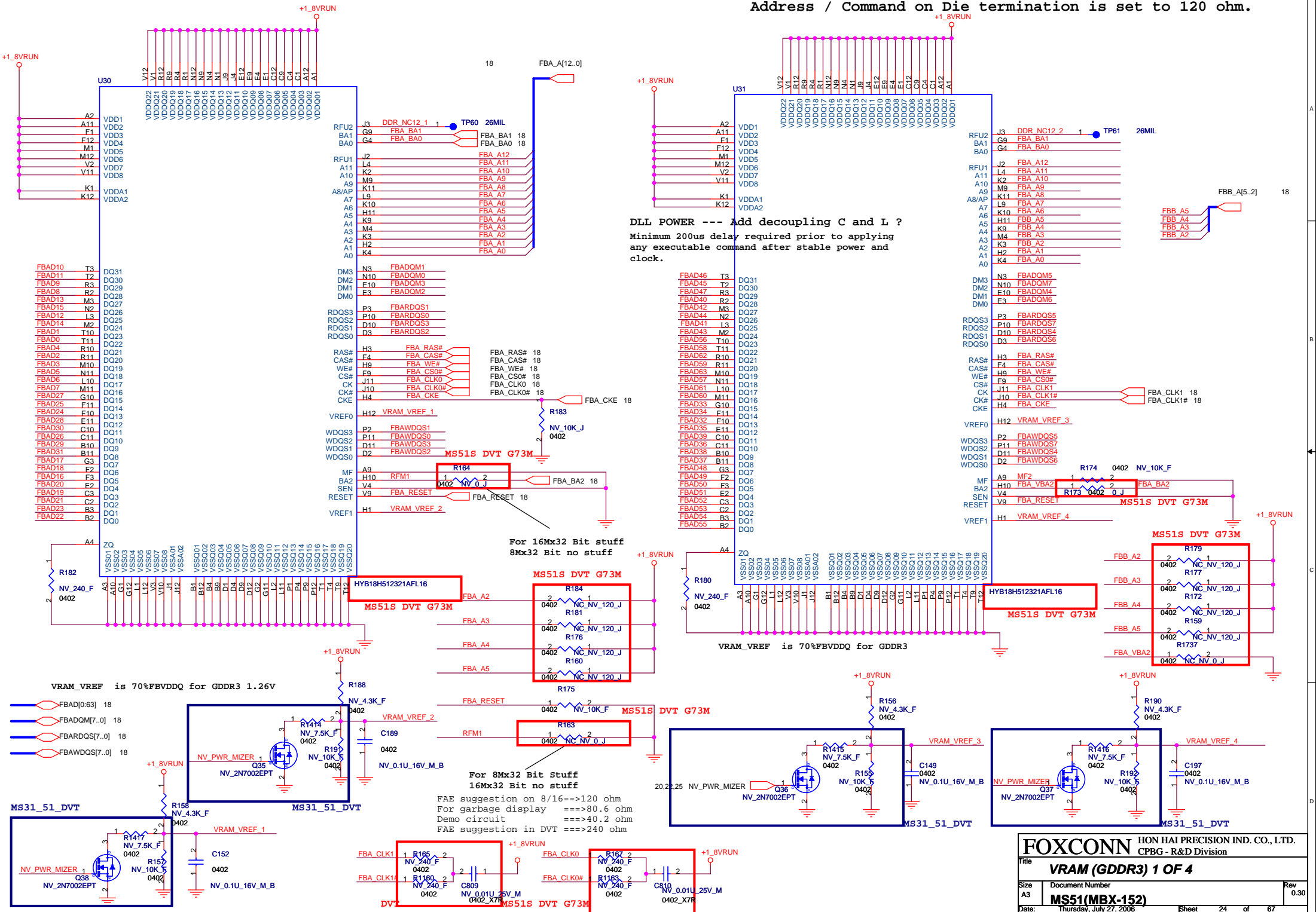
CLOSE TO GPU

DACA	VGA-CRT		I2CA
DACA-RED	R		
DACA-GREEN	G		
DACA-BLUE	B		
DACA-HSYNC	HSYNC		
DACA-VSYNC	VSYNC		
	VGA-DDOCCLK		SCL
	VGA-DDOCDATA		SDA
DACB	S-VIDEO	COMPOSITE	D-CONNECTOR
DACB-RED	C		PR
DACB-GREEN	Y		Y
DACB-BLUE		COMPOSITE	
			LINE1
			LINE2
			LINE3
			SCL
			SDA
DACC	DVI-I		I2CB
DACC-RED	R		
DACC-GREEN	G		
DACC-BLUE	B		
DACC-HSYNC	HSYNC		
DACC-VSYNC	VSYNC		
	DVI-DDOCCLK		SCL
	DVI-DDOCDATA		SDA



SF-GO7800-N-B1_B1

PVT MS51S DVT G73M



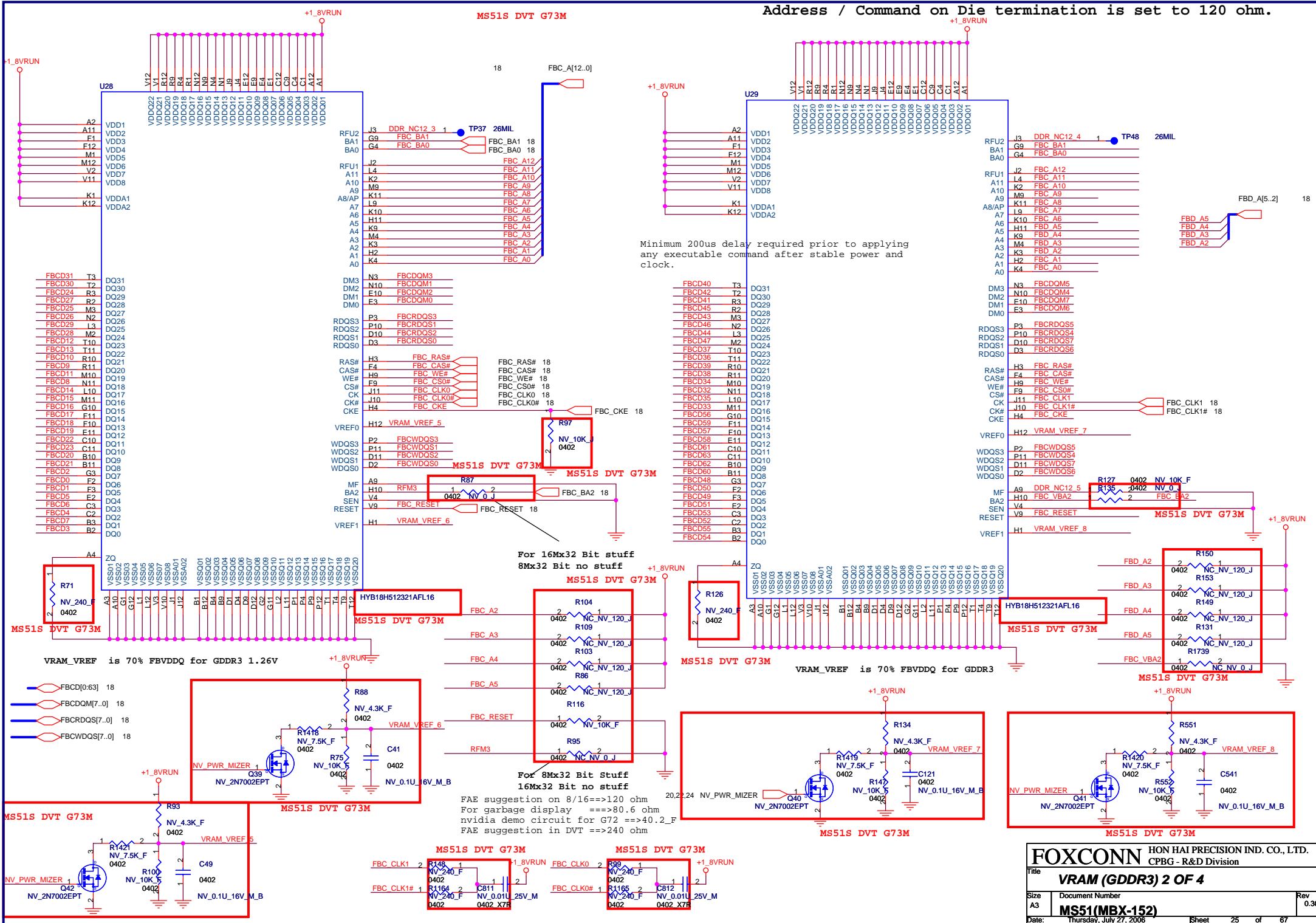
DLL POWER --- Add decoupling C and L ?
 Minimum 200us delay required prior to applying any executable command after stable power and clock.

For 16Mx32 Bit stuff
 8Mx32 Bit no stuff

VRAM_VREF is 70%FBVDDQ for GDDR3

VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V

For 8Mx32 Bit Stuff
 16Mx32 Bit no stuff
 FAE suggestion on 8/16==>120 ohm
 For garbage display ==>80.6 ohm
 Demo circuit ==>40.2 ohm
 FAE suggestion in DVT ==>24.0 ohm

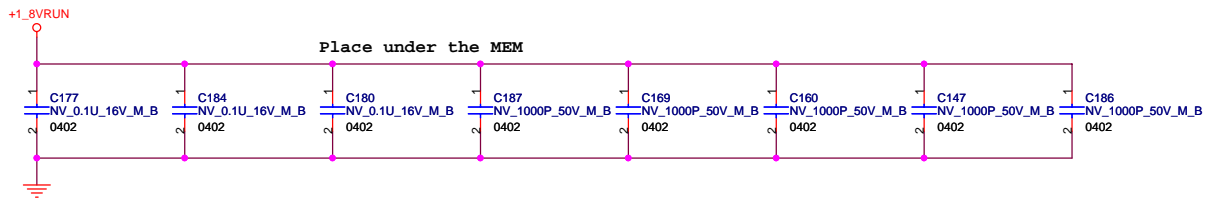
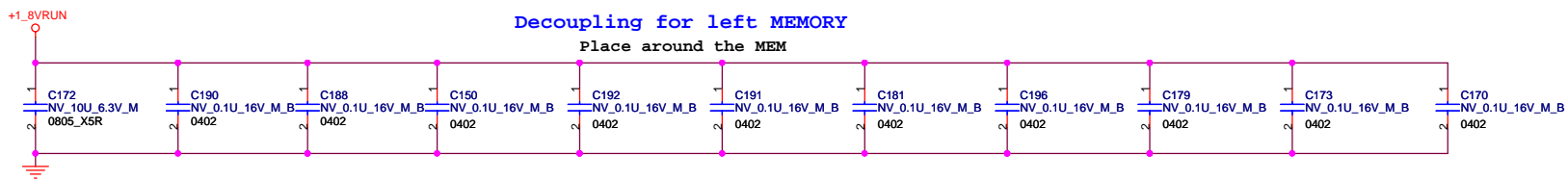
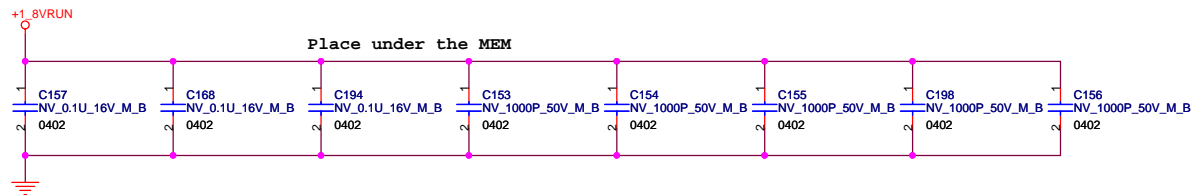
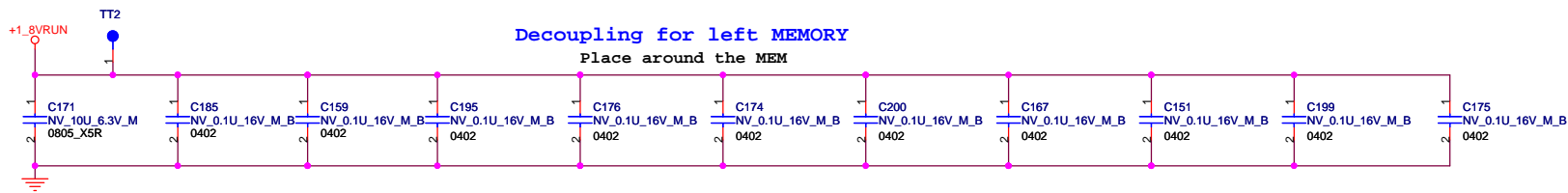


Minimum 200us delay required prior to applying any executable command after stable power and clock.

For 16Mx32 Bit stuff
8Mx32 Bit no stuff

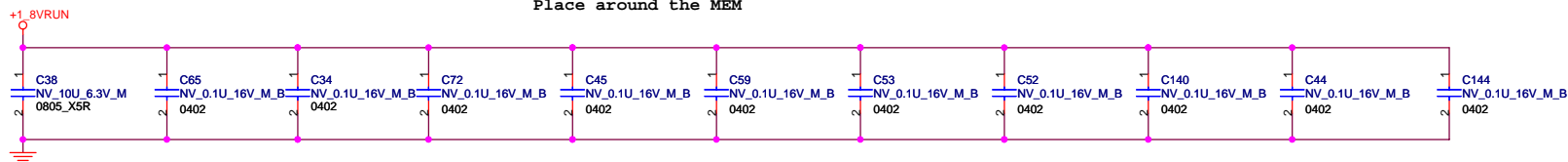
For 8Mx32 Bit Stuff
16Mx32 Bit no stuff

FAE suggestion on 8/16==>120 ohm
For garbage display ==>80.6 ohm
nvidea demo circuit for G72 ==>40.2 ohm
FAE suggestion in DVT ==>240 ohm



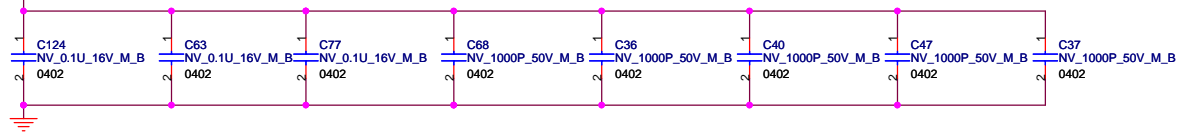
Decoupling for right MEMORY

Place around the MEM



+1.8VRUN 1.2A

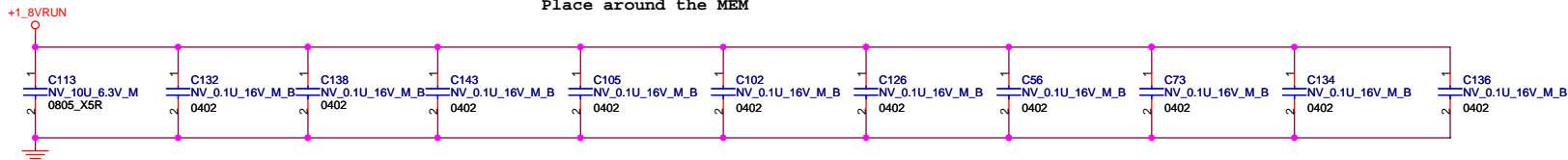
Place under the MEM



NO USE

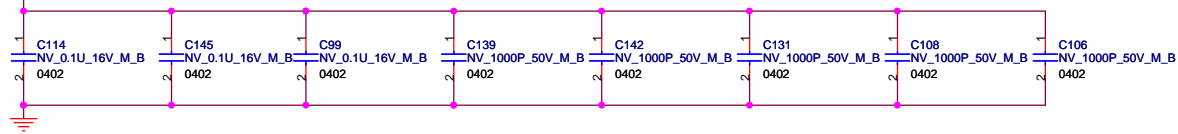
Decoupling for right MEMORY

Place around the MEM



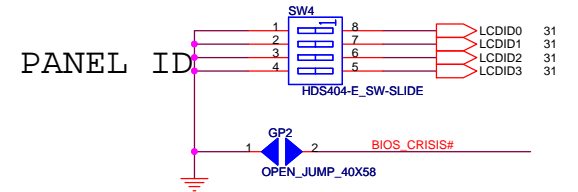
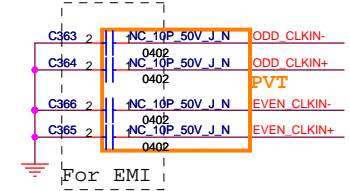
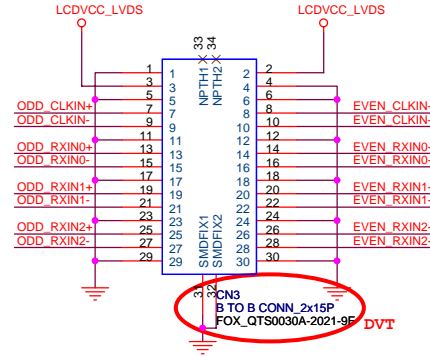
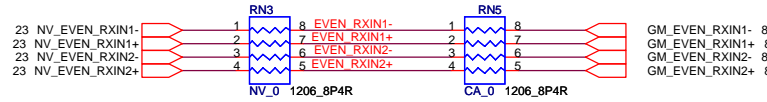
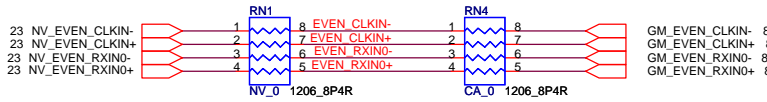
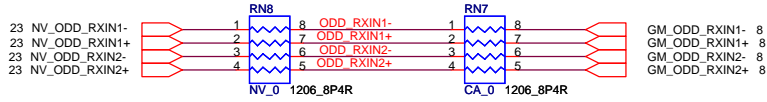
+1.8VRUN 1.2A

Place under the MEM



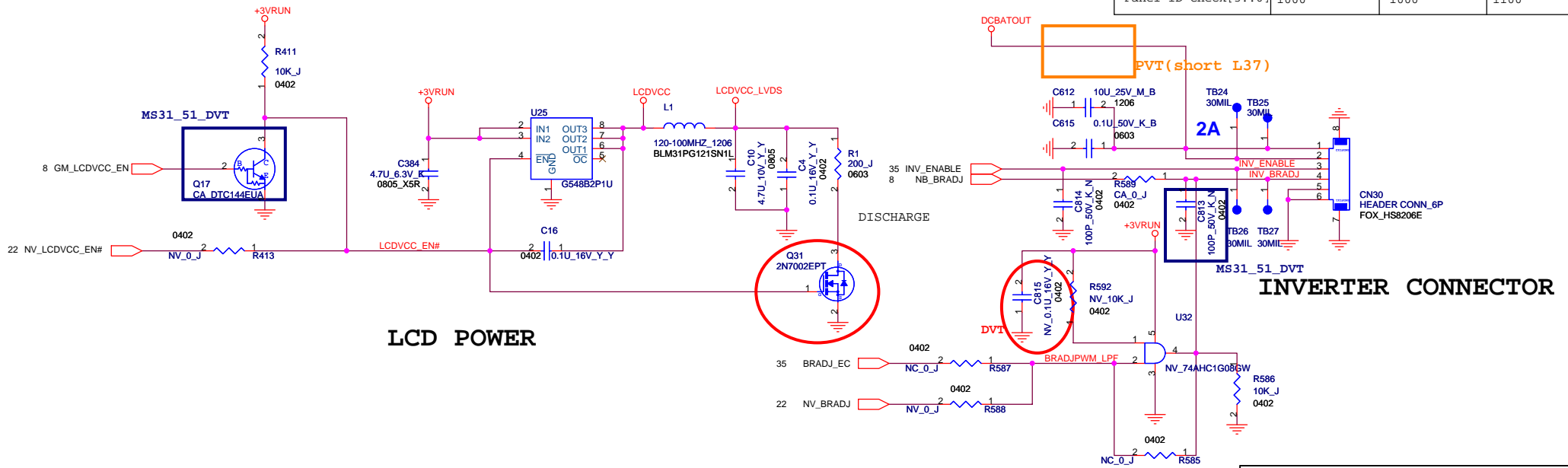
MS51S DVT G73M

LVDS



Type	WXGA	WXGA-HC	WSXGA+
Size	15.4" wide	15.4" wide	15.4" wide
Vendor	Hitachi	Hitachi	Hitachi
Device Name	TX39D81VC1AAA	TX39D80VC1GAA	TX39D90VC1GAA
Panel ID check[3..0]	1000	1000	1100

LVDS CONNECTOR



LCD POWER

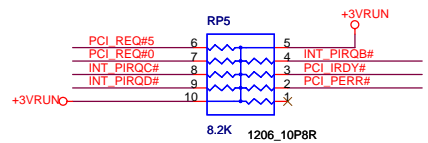
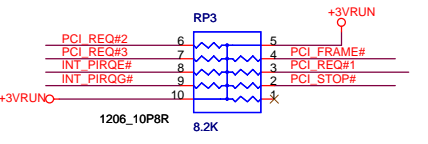
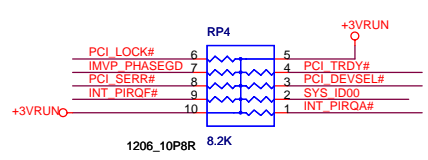
INVERTER CONNECTOR

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CPBG - R&D Division

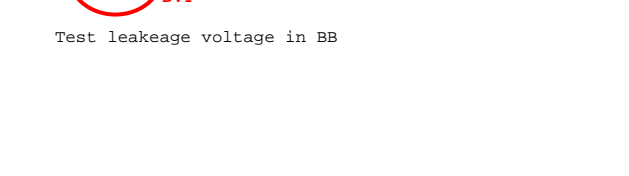
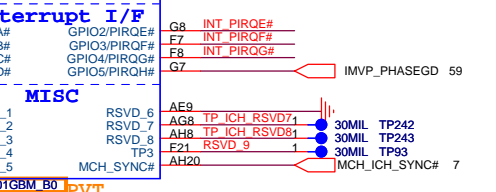
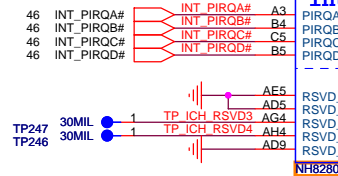
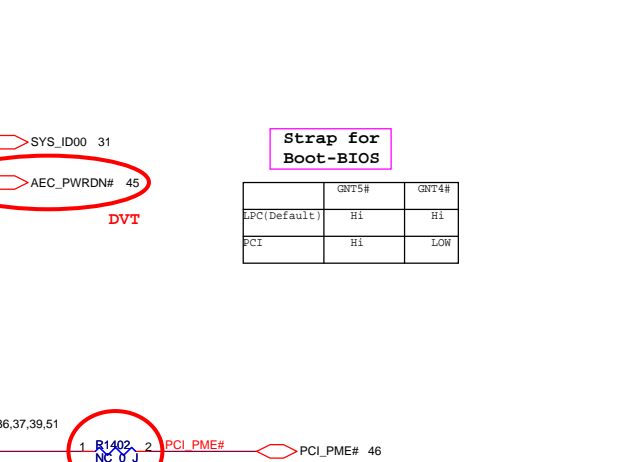
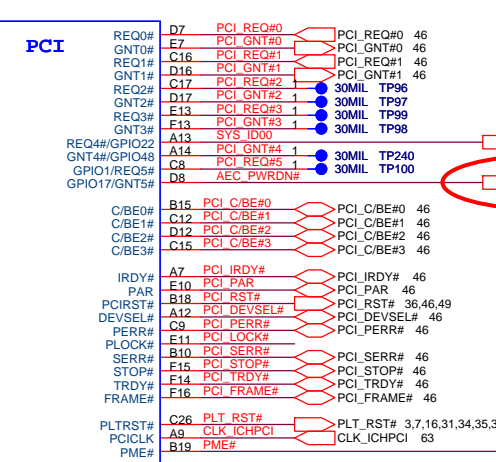
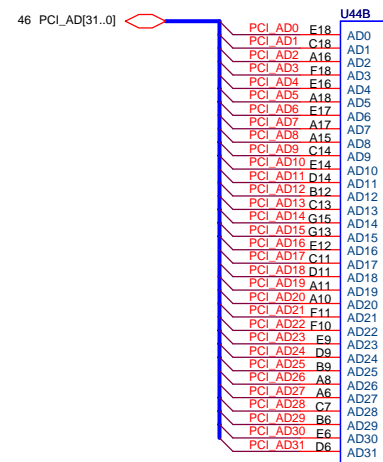
Title: **LVDS**

Size A3 Document Number: **MS51(MBX-152)** Rev 0.30

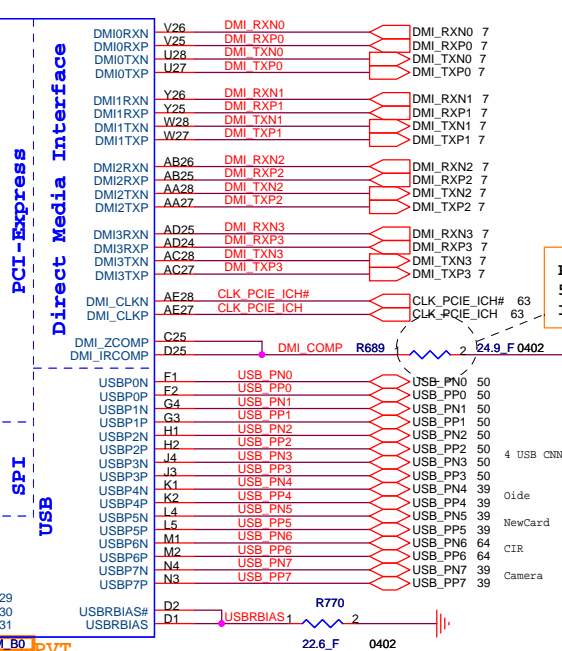
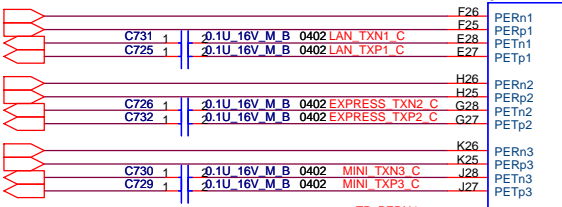
Date: Thursday, July 27, 2006 Sheet 28 of 67



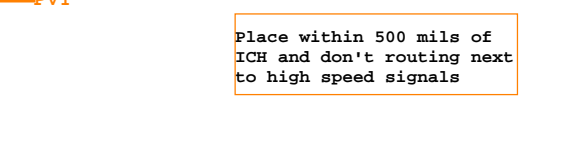
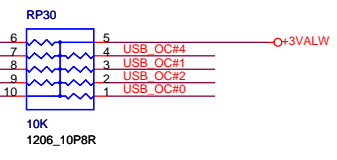
PCI Pullups



- 51 LAN_RXN1
- 51 LAN_RXP1
- 51 LAN_TXN1
- 51 LAN_TXP1
- 39 EXPRESS_RXN2
- 39 EXPRESS_RXP2
- 39 EXPRESS_TXN2
- 39 EXPRESS_TXP2
- 37 MINI_RXN3
- 37 MINI_RXP3
- 37 MINI_TXN3
- 37 MINI_TXP3



Place within 500 mils of ICH



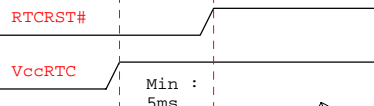
Place within 500 mils of ICH and don't routing next to high speed signals

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CPBG - R&D Division

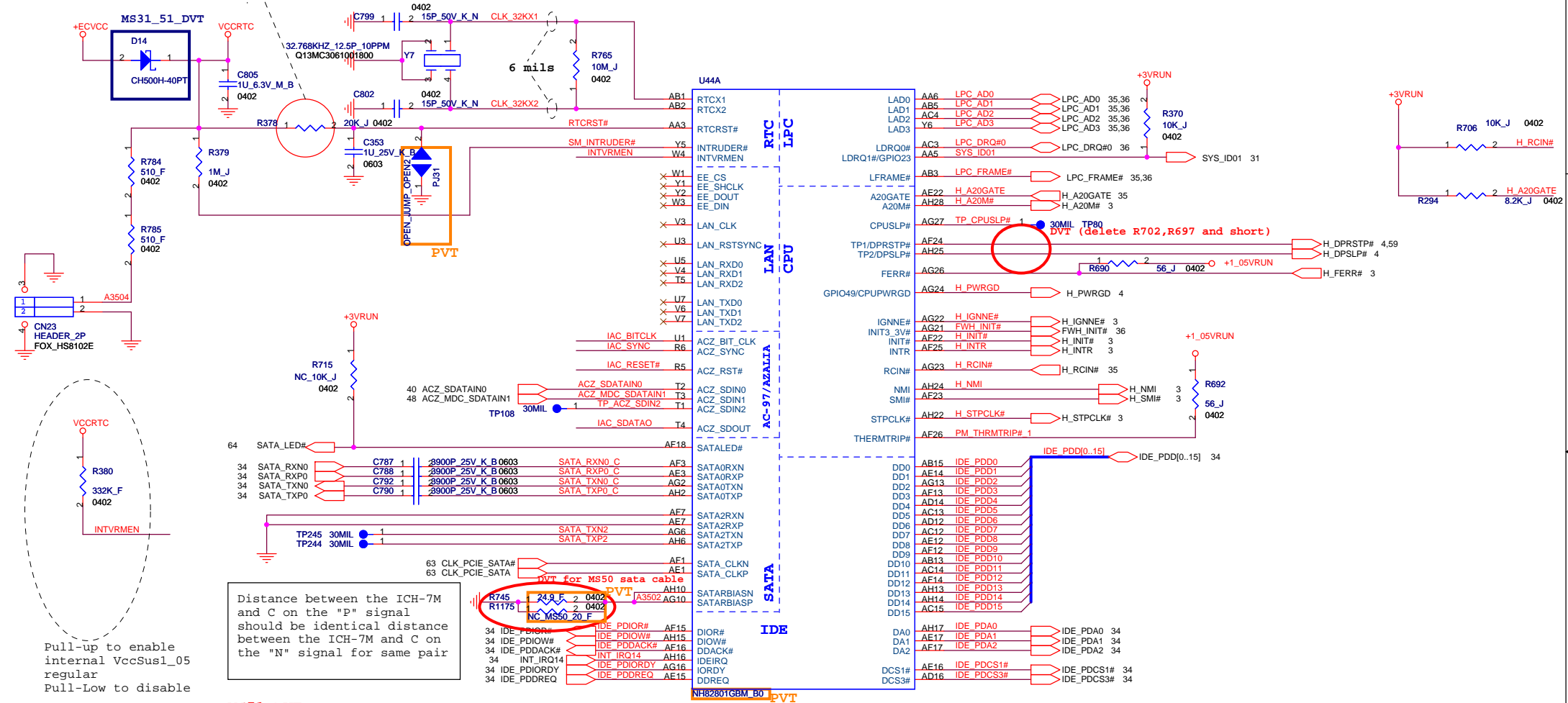
Title: **ICH7-M(PCI/DMI/USB/PCIE) 1/5**

Size A3 Document Number: **MS51(MBX-152)** Rev 0.30

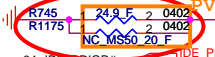
Date: Thursday, July 27, 2006 Sheet 29 of 67



The traces inside this block should be wider.
No digital signals routed under XTAL

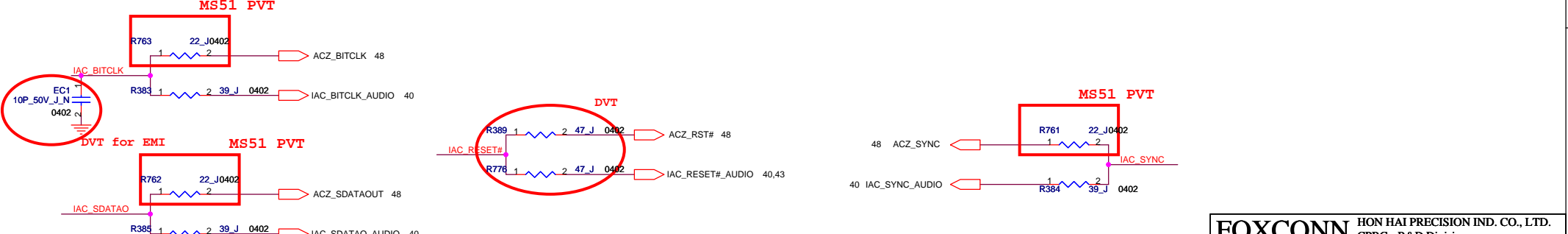


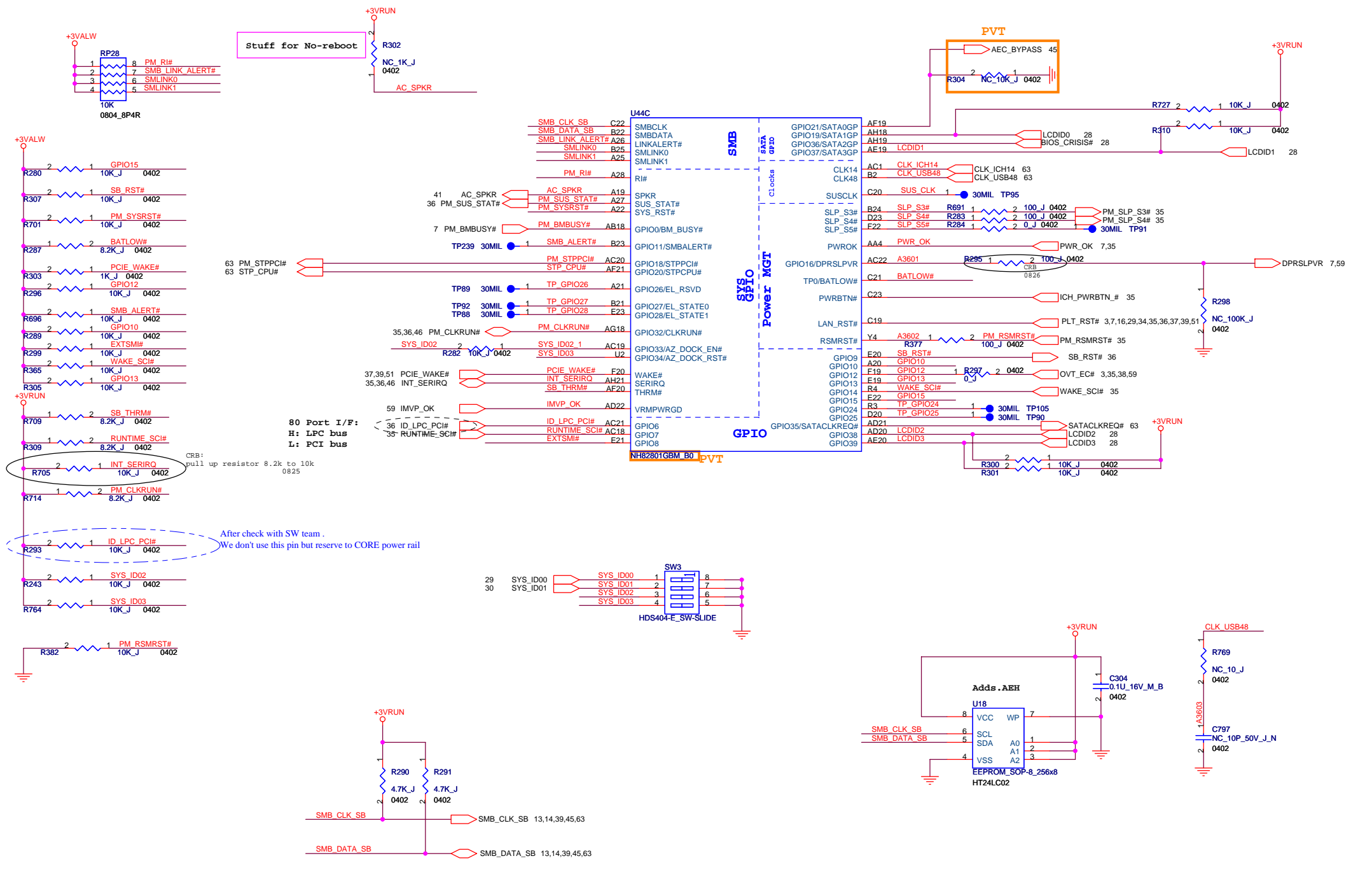
Distance between the ICH-7M and C on the "P" signal should be identical distance between the ICH-7M and C on the "N" signal for same pair

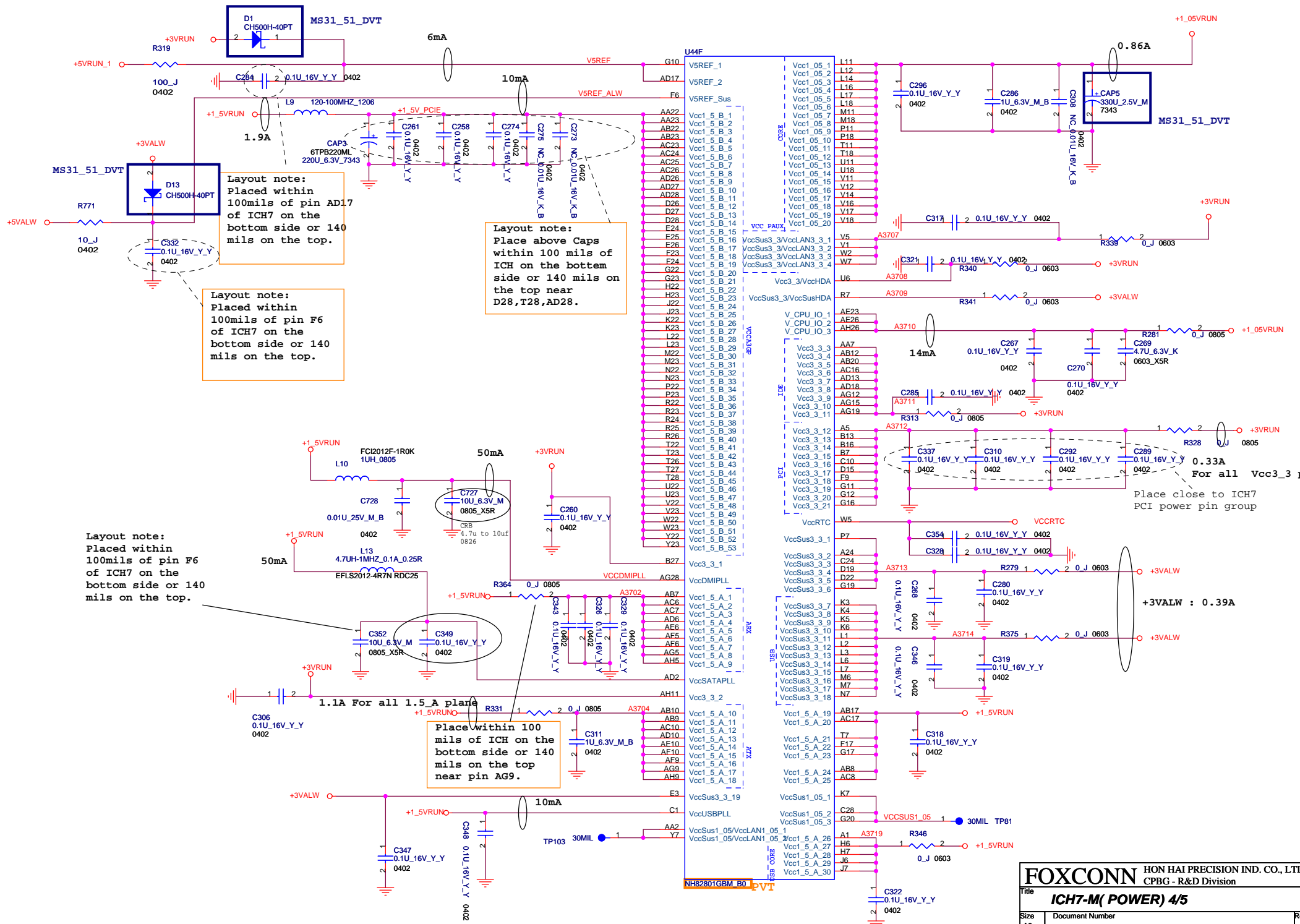


Pull-up to enable internal VccSus1_05 regular
Pull-Low to disable

MS51 PVT







Layout note:
Placed within 100mils of pin AD1.7 of ICH7 on the bottom side or 140mils on the top.

Layout note:
Placed within 100mils of pin F6 of ICH7 on the bottom side or 140mils on the top.

Layout note:
Place above Caps within 100mils of ICH on the bottom side or 140mils on the top near D28, T28, AD28.

Layout note:
Placed within 100mils of pin F6 of ICH7 on the bottom side or 140mils on the top.

Layout note:
Place within 100mils of ICH on the bottom side or 140mils on the top near pin AG9.

Place close to ICH7 PCI power pin group

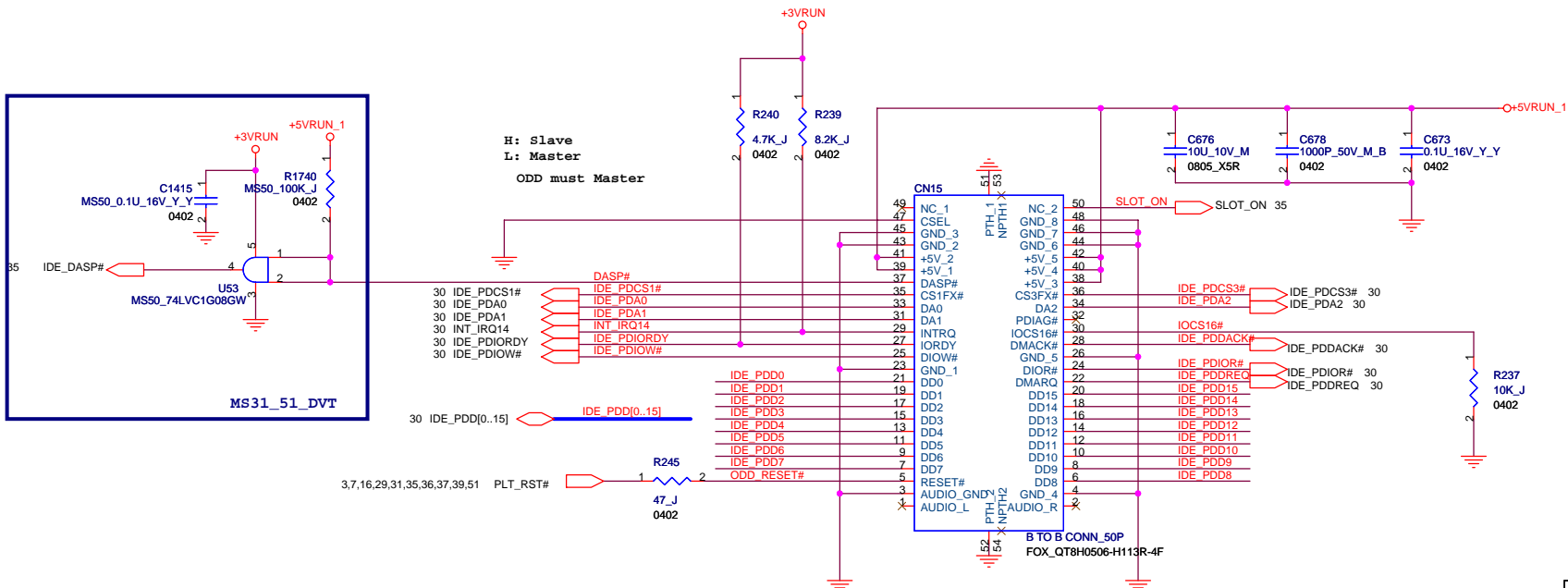
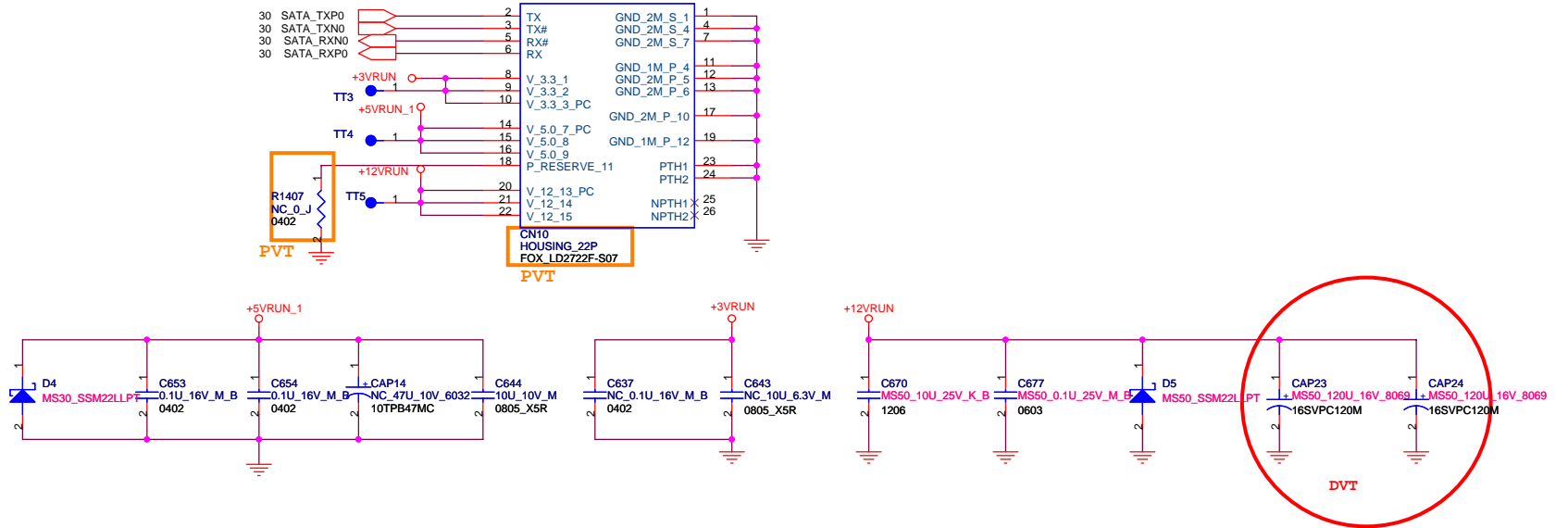
+3VALW : 0.39A

U44E			
A4	VSS_1	VSS_98	P28
A23	VSS_2	VSS_99	R1
B1	VSS_3	VSS_100	R11
B8	VSS_4	VSS_101	R12
B11	VSS_5	VSS_102	R13
B14	VSS_6	VSS_103	R14
B17	VSS_7	VSS_104	R15
B20	VSS_8	VSS_105	R16
B26	VSS_9	VSS_106	R17
B28	VSS_10	VSS_107	R18
C2	VSS_11	VSS_108	T6
C6	VSS_12	VSS_109	T12
C27	VSS_13	VSS_110	T13
D10	VSS_14	VSS_111	T14
D13	VSS_15	VSS_112	T15
D18	VSS_16	VSS_113	T16
D21	VSS_17	VSS_114	T17
D24	VSS_18	VSS_115	U4
E1	VSS_19	VSS_116	U12
E2	VSS_20	VSS_117	U13
F4	VSS_21	VSS_118	U14
F8	VSS_22	VSS_119	U15
F15	VSS_23	VSS_120	U16
F3	VSS_24	VSS_121	U17
F4	VSS_25	VSS_122	U24
F5	VSS_26	VSS_123	U25
F12	VSS_27	VSS_124	U26
F27	VSS_28	VSS_125	V2
F28	VSS_29	VSS_126	V13
G1	VSS_30	VSS_127	V15
G2	VSS_31	VSS_128	V24
G5	VSS_32	VSS_129	V27
G6	VSS_33	VSS_130	V28
G9	VSS_34	VSS_131	W6
G14	VSS_35	VSS_132	W24
G18	VSS_36	VSS_133	W25
G21	VSS_37	VSS_134	W26
G24	VSS_38	VSS_135	Y3
G25	VSS_39	VSS_136	Y24
G26	VSS_40	VSS_137	Y27
H3	VSS_41	VSS_138	Y28
H4	VSS_42	VSS_139	AA1
H5	VSS_43	VSS_140	AA24
H24	VSS_44	VSS_141	AA25
H27	VSS_45	VSS_142	AA26
H28	VSS_46	VSS_143	AB4
J1	VSS_47	VSS_144	AB6
J2	VSS_48	VSS_145	AB11
J5	VSS_49	VSS_146	AB14
J24	VSS_50	VSS_147	AB16
J25	VSS_51	VSS_148	AB19
J26	VSS_52	VSS_149	AB21
K24	VSS_53	VSS_150	AB24
K27	VSS_54	VSS_151	AB27
K28	VSS_55	VSS_152	AB28
L13	VSS_56	VSS_153	AC2
L15	VSS_57	VSS_154	AC5
L24	VSS_58	VSS_155	AC9
L25	VSS_59	VSS_156	AC11
L26	VSS_60	VSS_157	AD1
M3	VSS_61	VSS_158	AD3
M4	VSS_62	VSS_159	AD4
M5	VSS_63	VSS_160	AD7
M12	VSS_64	VSS_161	AD8
M13	VSS_65	VSS_162	AD11
M14	VSS_66	VSS_163	AD15
M15	VSS_67	VSS_164	AD19
M16	VSS_68	VSS_165	AD23
M17	VSS_69	VSS_166	AE2
M24	VSS_70	VSS_167	AE4
M27	VSS_71	VSS_168	AE8
M28	VSS_72	VSS_169	AE11
N1	VSS_73	VSS_170	AE13
N2	VSS_74	VSS_171	AE18
N5	VSS_75	VSS_172	AE21
N6	VSS_76	VSS_173	AE24
N11	VSS_77	VSS_174	AE25
N12	VSS_78	VSS_175	AF2
N13	VSS_79	VSS_176	AF4
N14	VSS_80	VSS_177	AF8
N15	VSS_81	VSS_178	AF11
N16	VSS_82	VSS_179	AF27
N17	VSS_83	VSS_180	AF28
N18	VSS_84	VSS_181	AG1
N24	VSS_85	VSS_182	AG3
N25	VSS_86	VSS_183	AG7
N26	VSS_87	VSS_184	AG11
P3	VSS_88	VSS_185	AG14
P4	VSS_89	VSS_186	AG17
P12	VSS_90	VSS_187	AG20
P13	VSS_91	VSS_188	AG25
P14	VSS_92	VSS_189	AH1
P15	VSS_93	VSS_190	AH3
P16	VSS_94	VSS_191	AH7
P17	VSS_95	VSS_192	AH12
P24	VSS_96	VSS_193	AH23
P27	VSS_97	VSS_194	AH27

NH82801GBM_B0 PVT

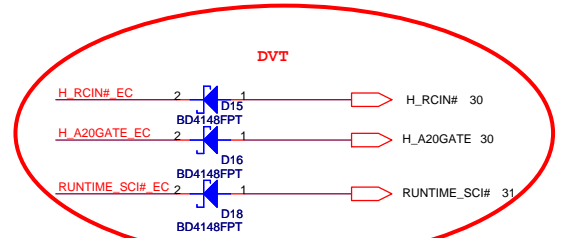
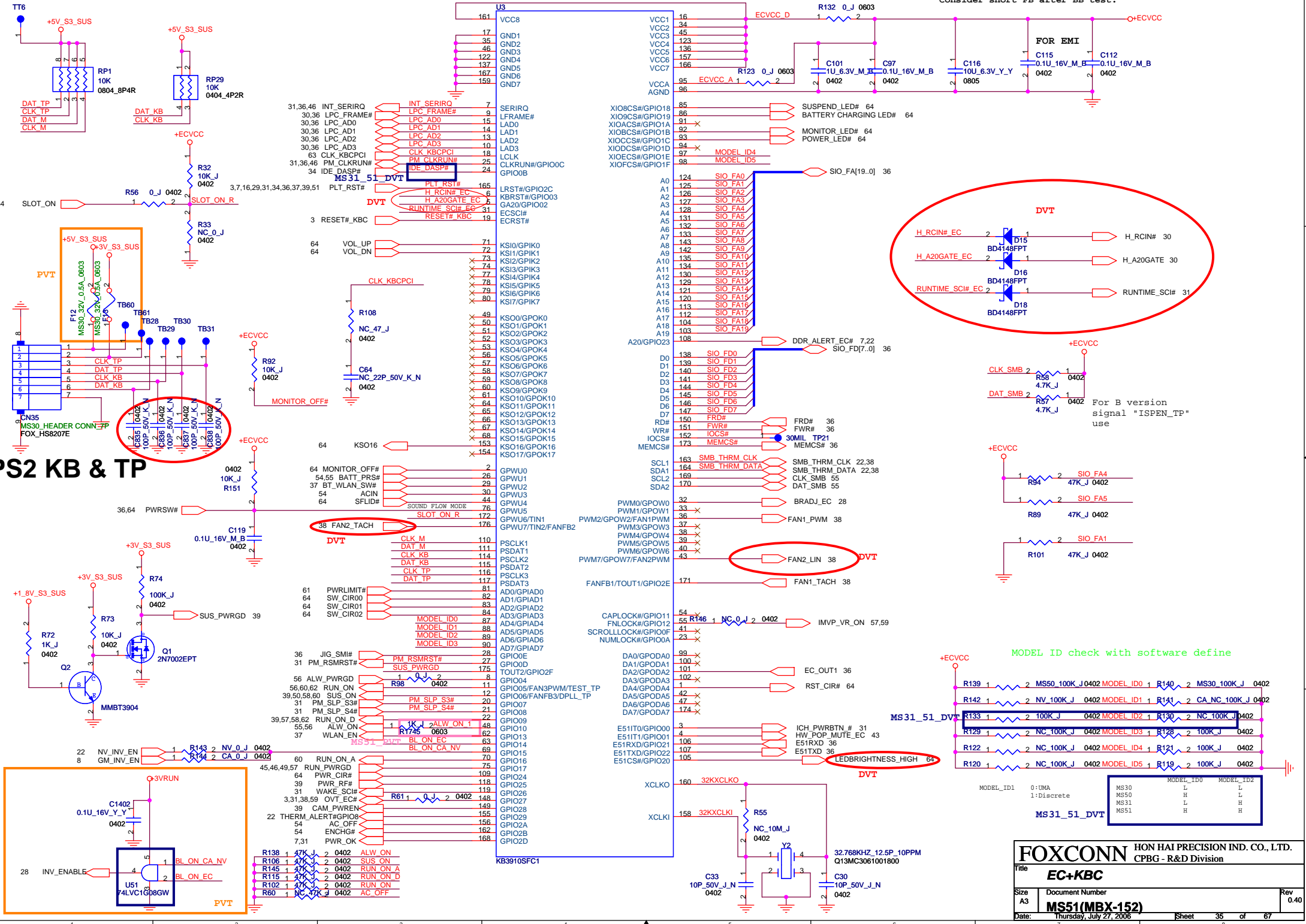
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Title	ICH7-M (GND) 5/5	
Size	Document Number	Rev
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SATA HDD CONN

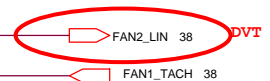
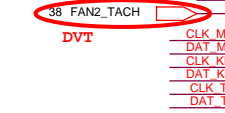
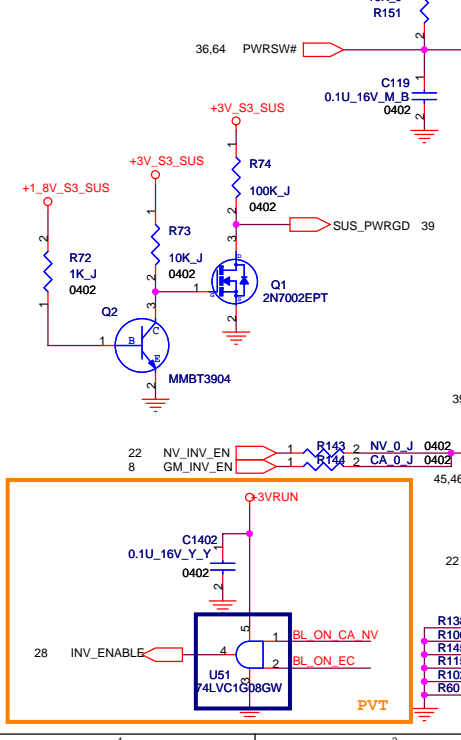


CD-ROM CONN

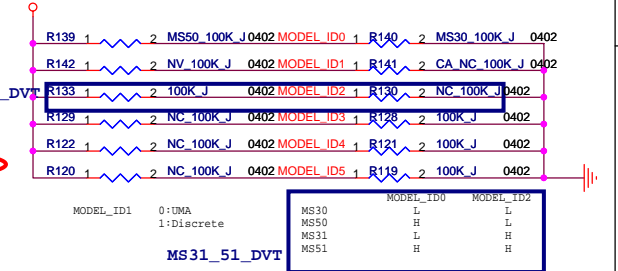
Consider short FB after BB test.



PS2 KB & TP

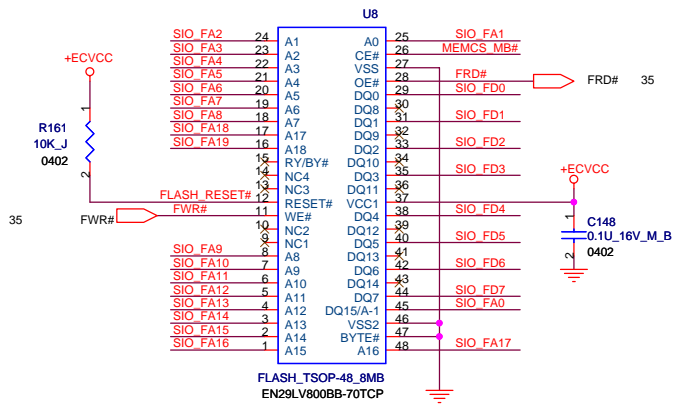


MODEL ID check with software define

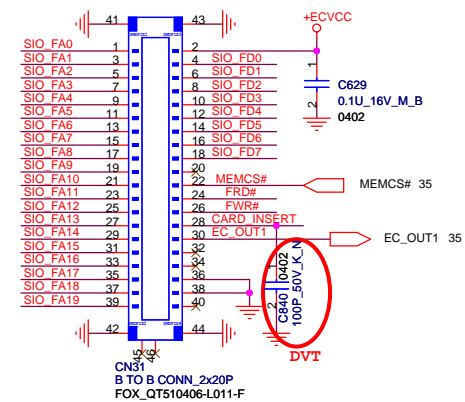
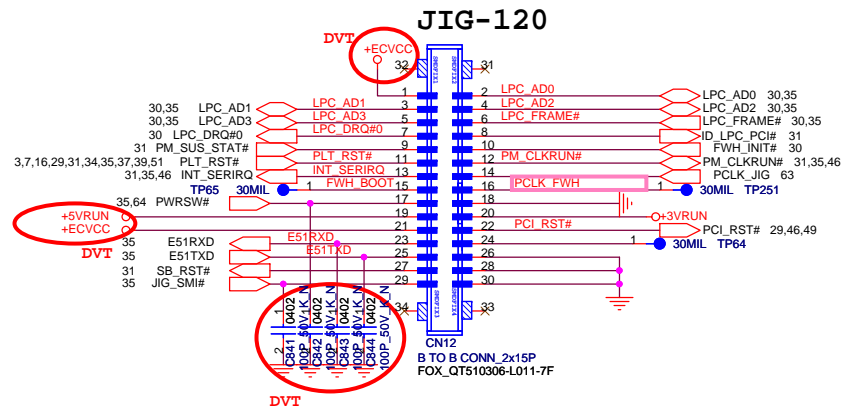
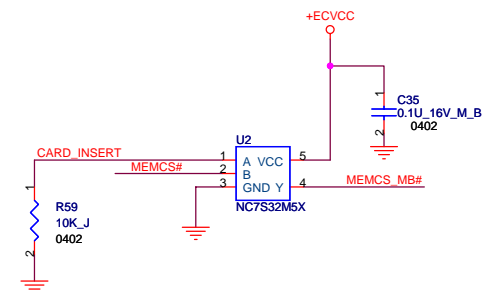


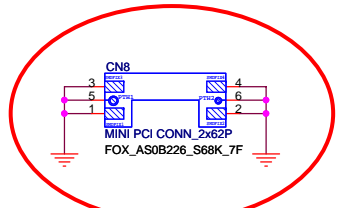
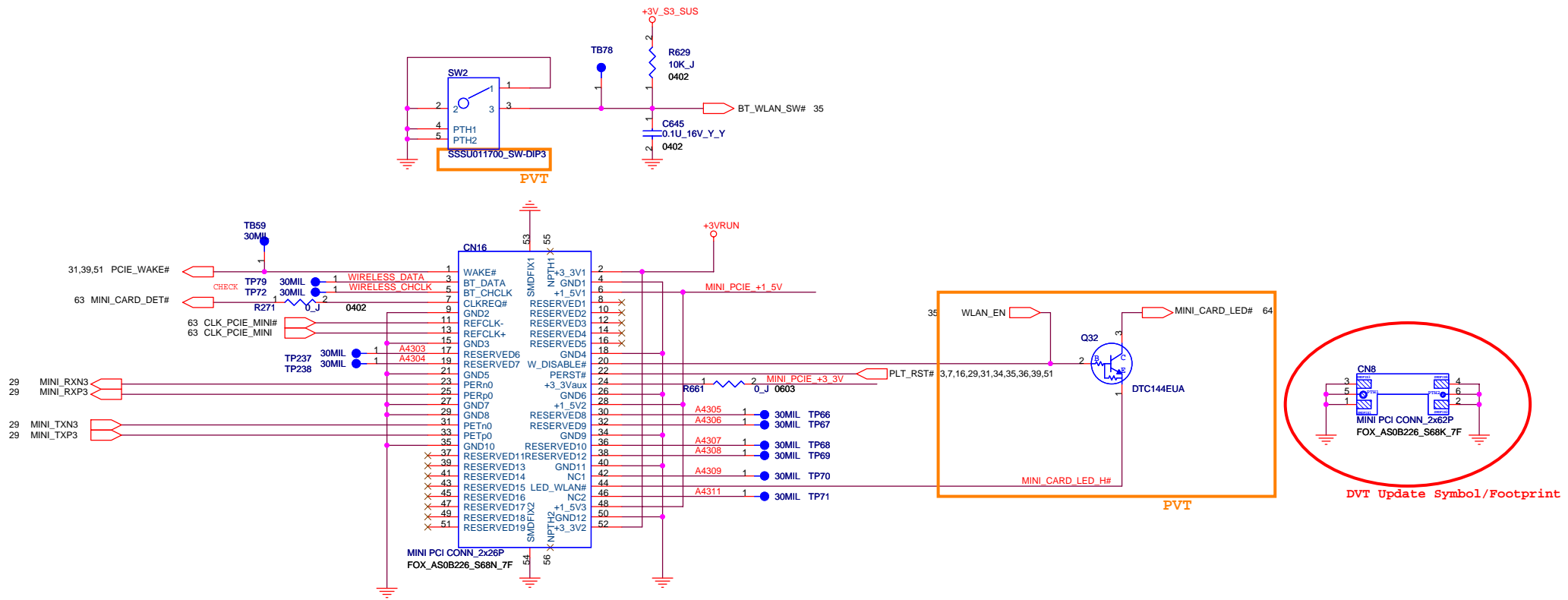
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CPBG - R&D Division	
Title: EC+KBC	
Size: A3	Document Number: MS51(MBX-152)
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35 SIO_FA[19..0]
35 SIO_FD[7..0]

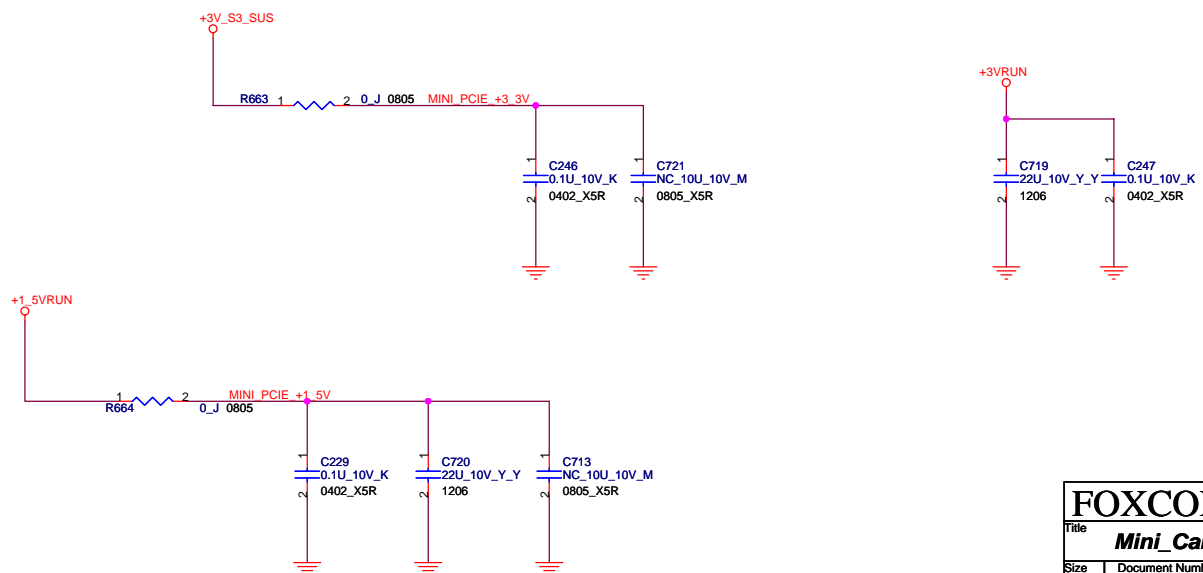


BIOS ROM

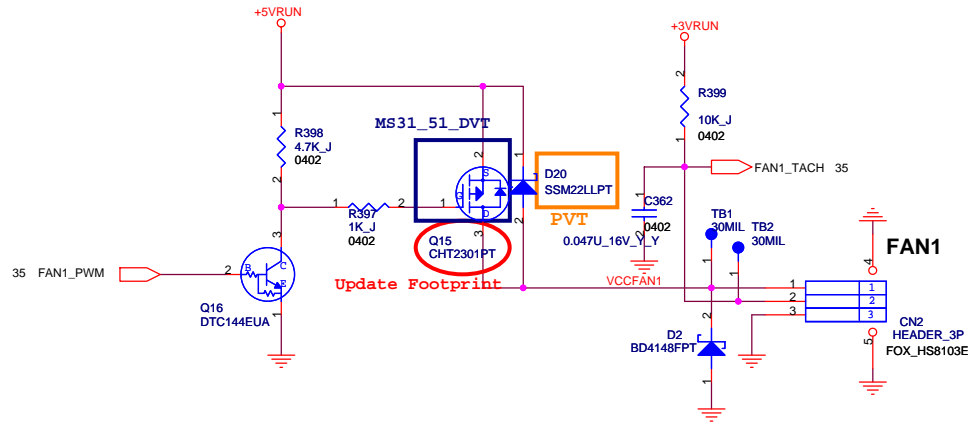




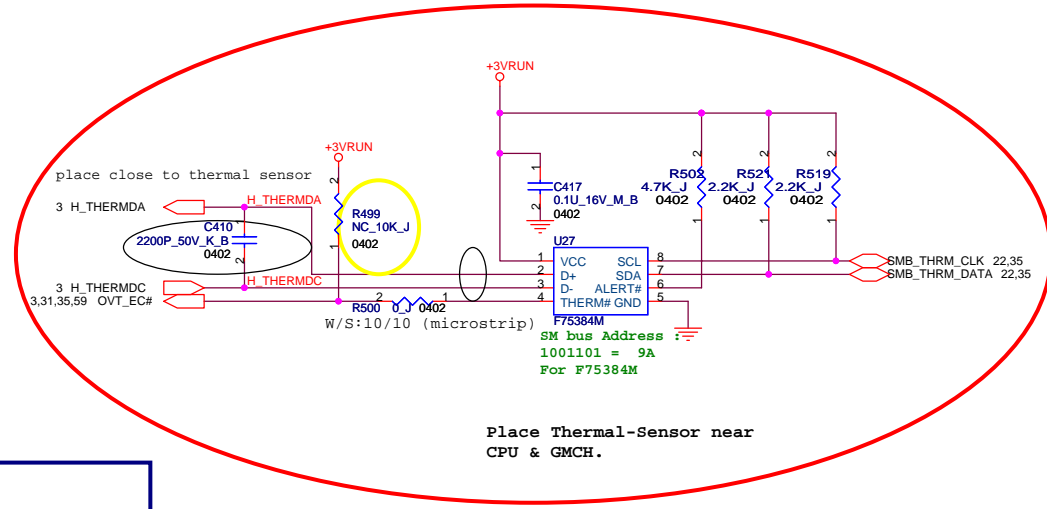
DVT Update Symbol/Footprint



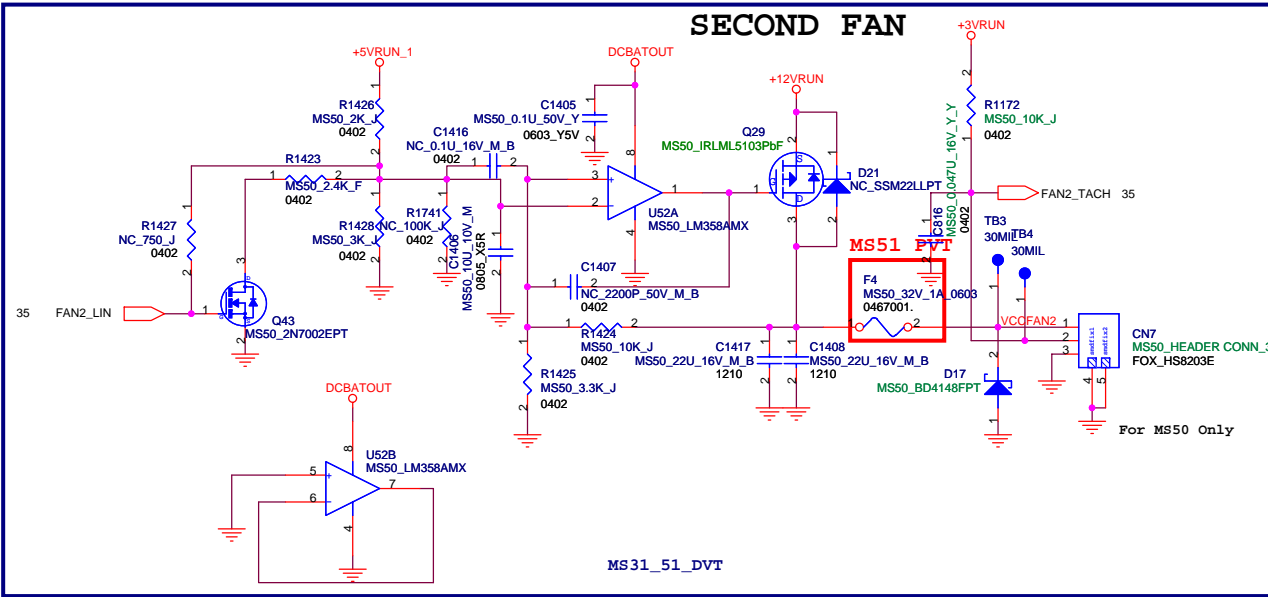
FAN



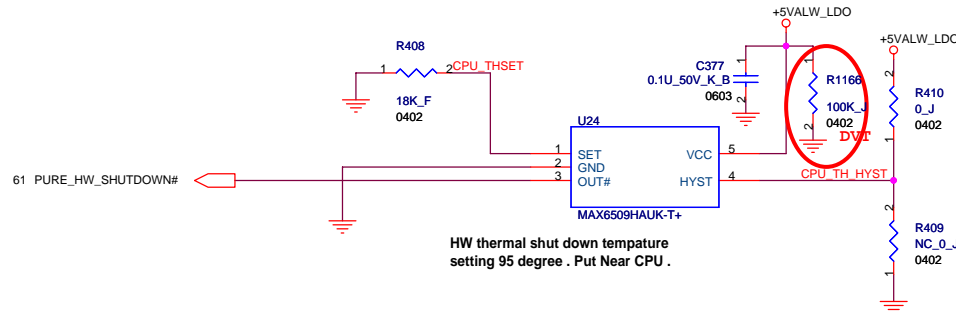
CPU SENSOR



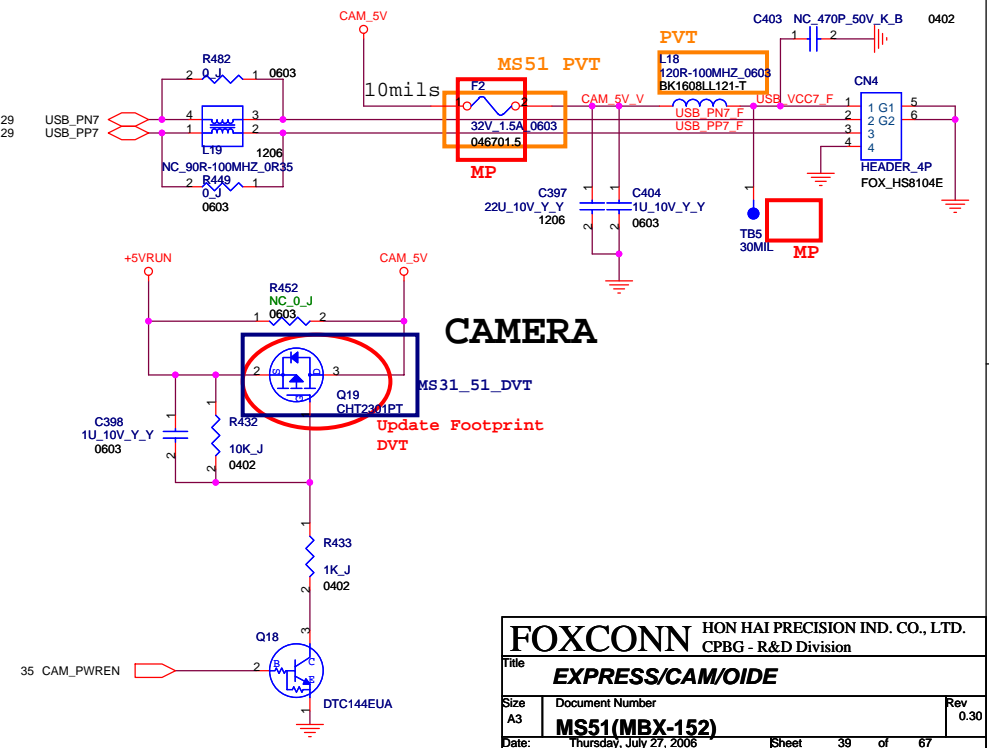
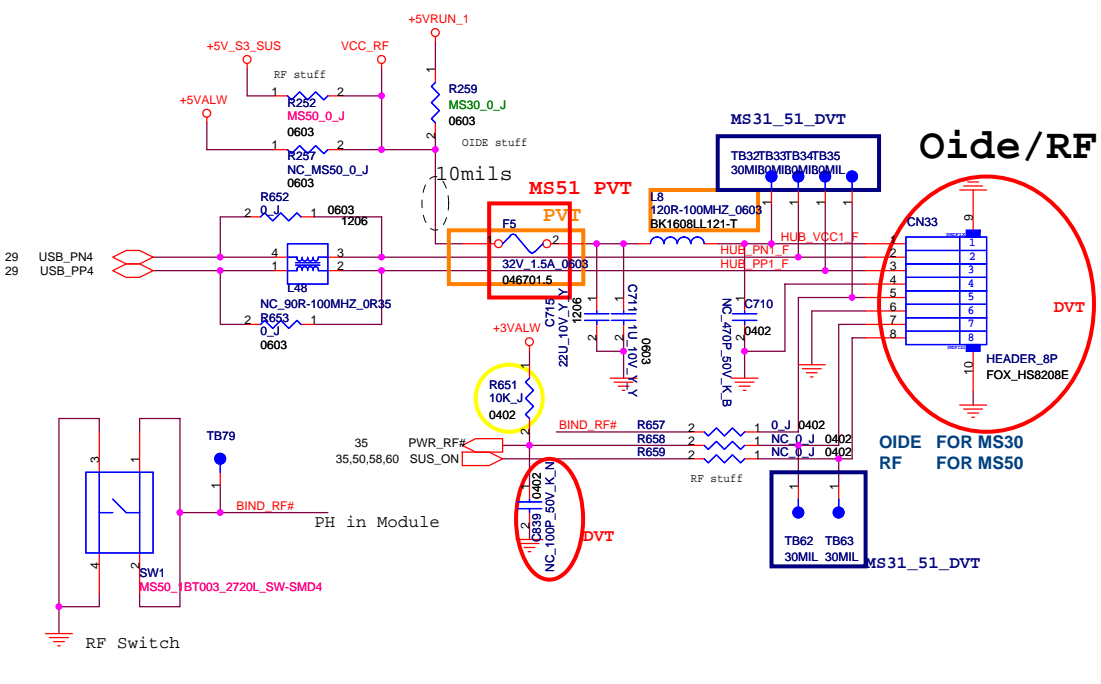
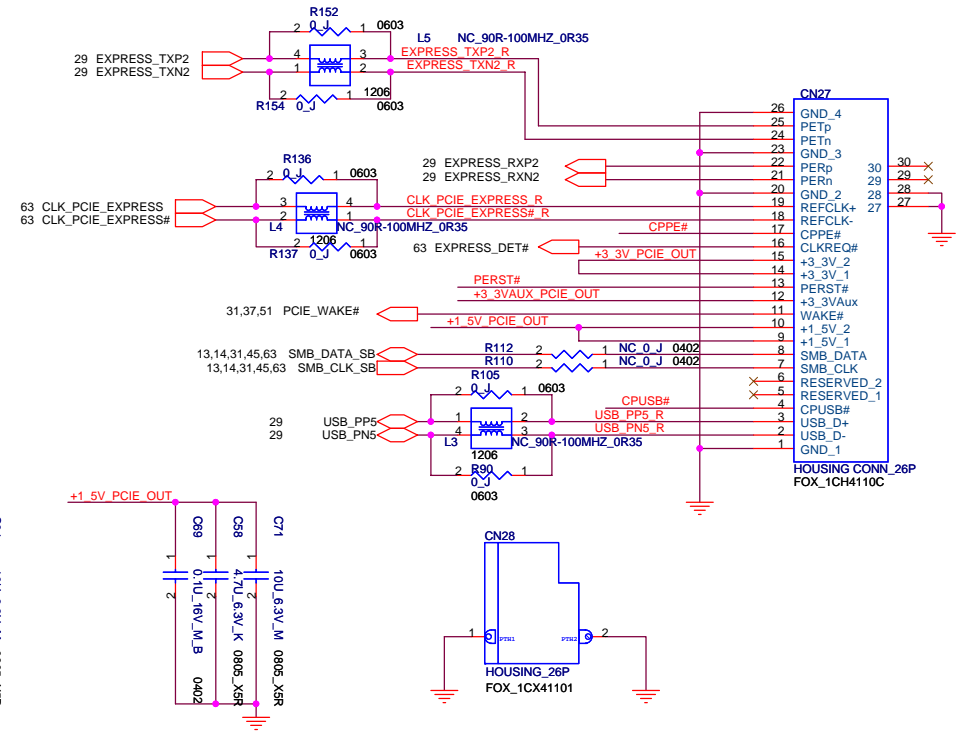
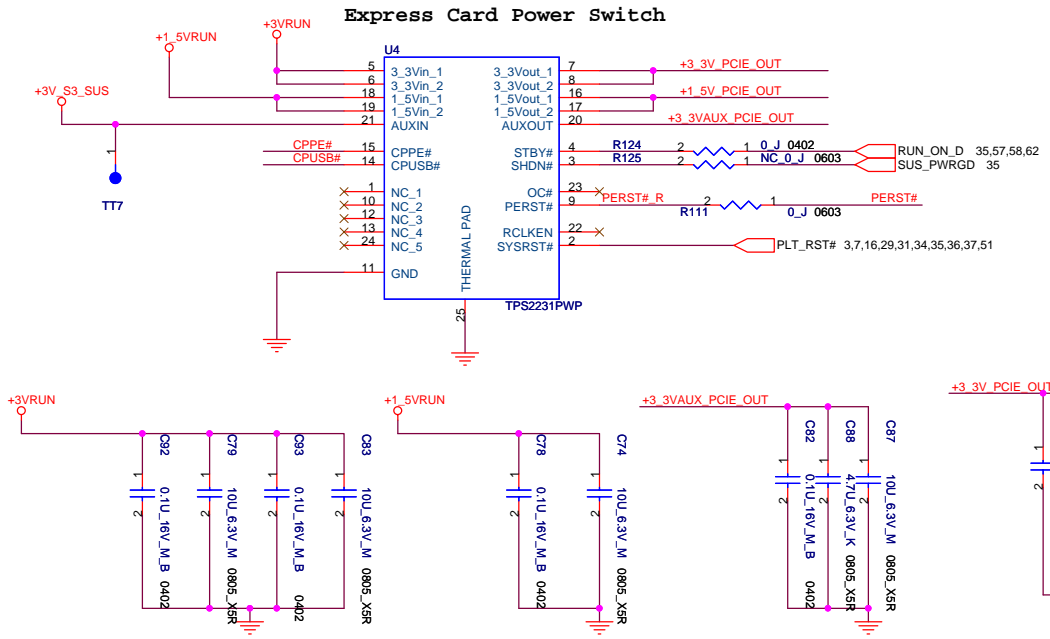
SECOND FAN

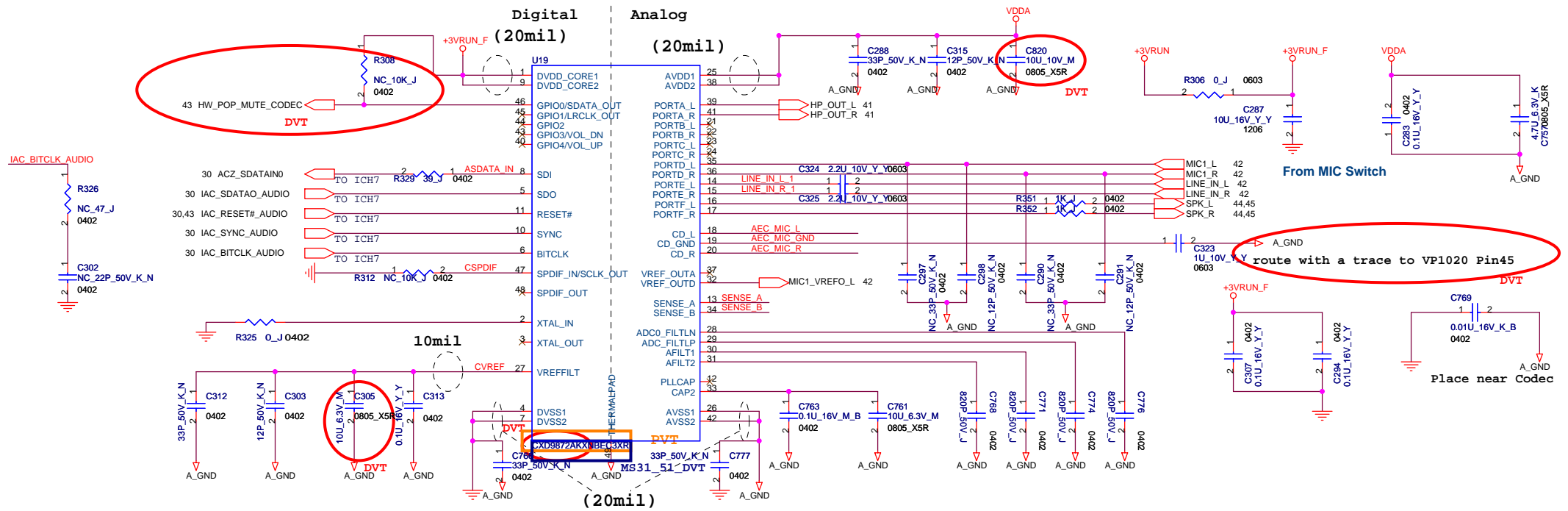


HW THERMAL PROTECTION

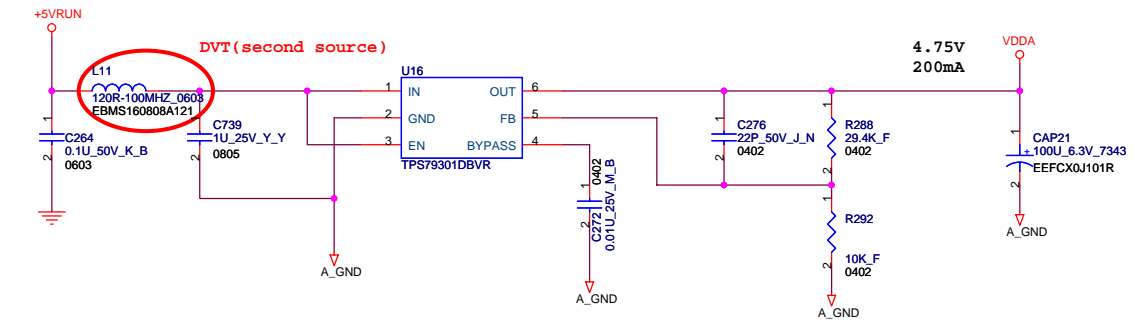
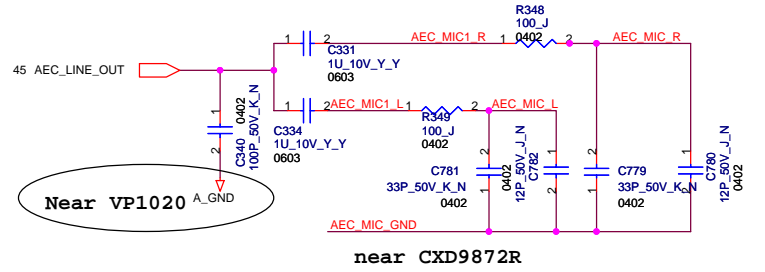
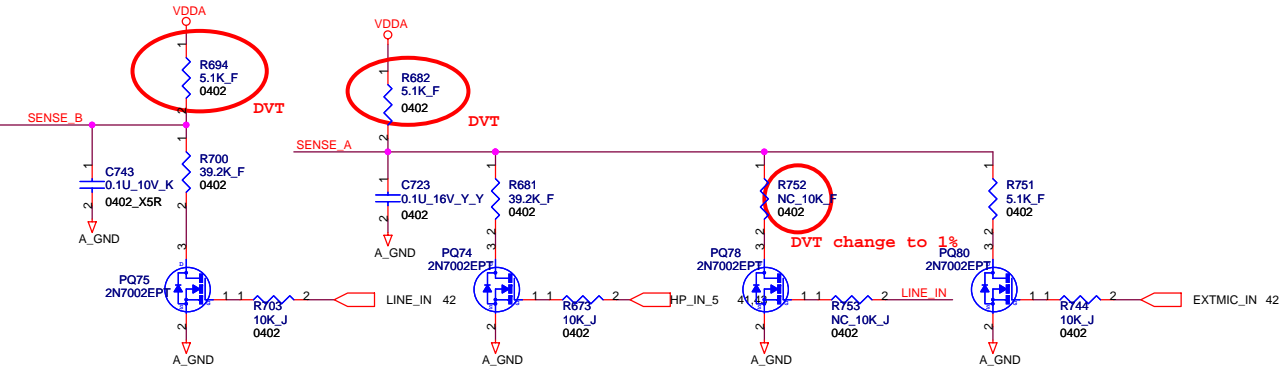


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CPBG - R&D Division	
FAN/HW THERMAL PROTECT	
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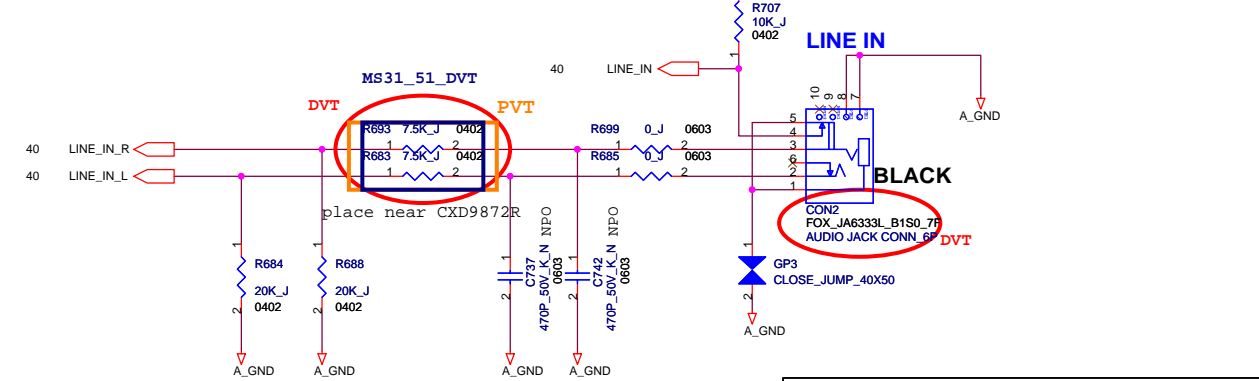
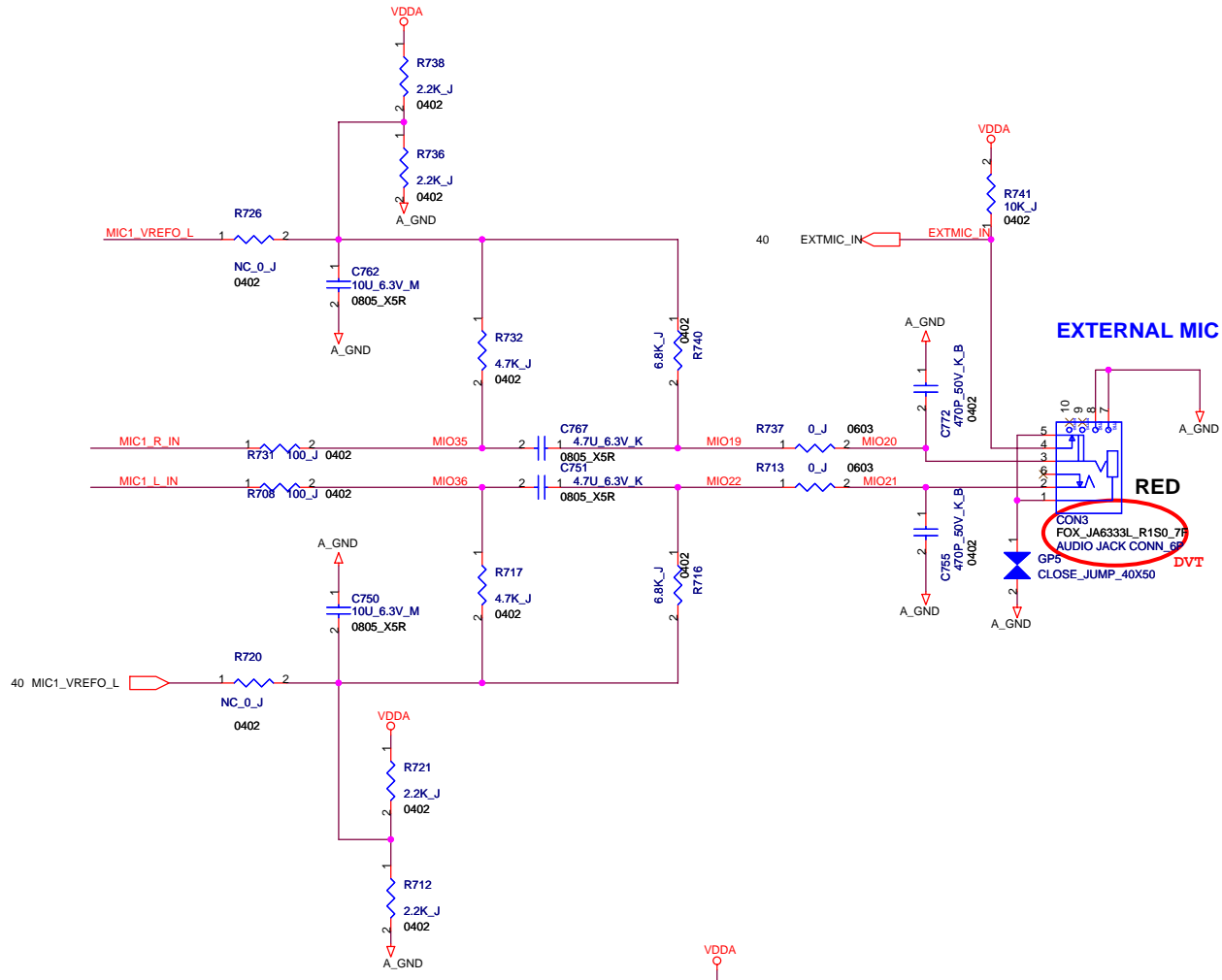
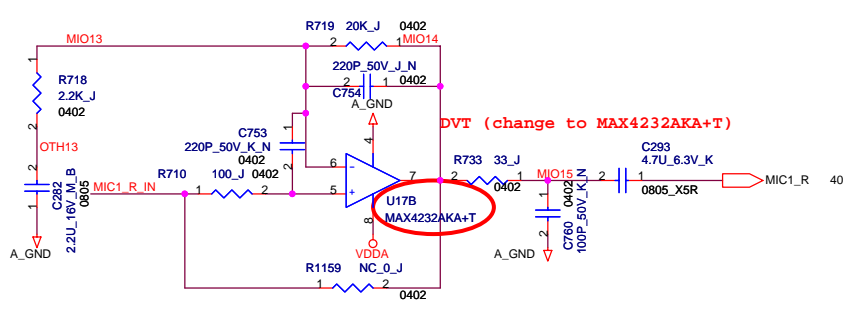
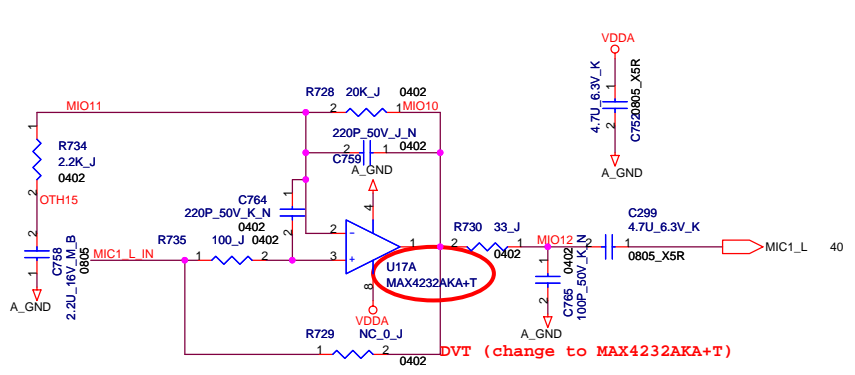


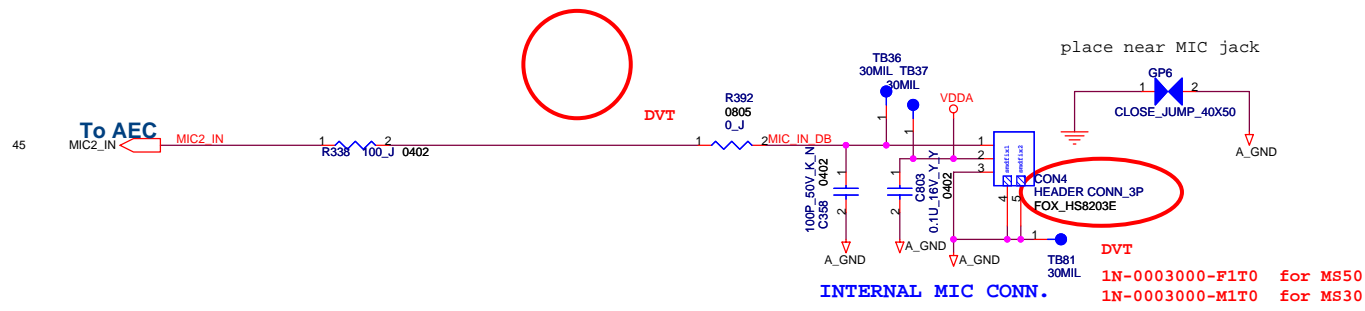
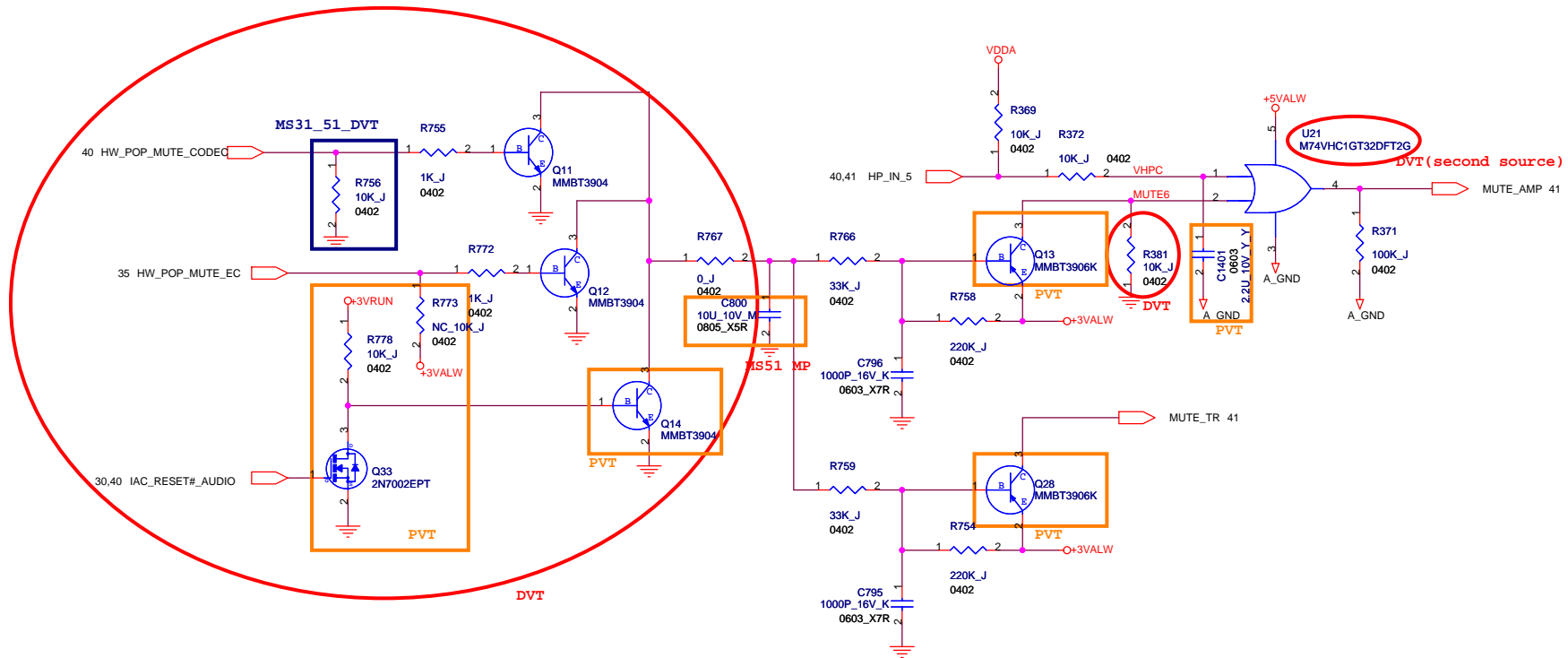
R692, C723 put near SENSE_A(pin13)
R694, C743 put near SENSE_B(pin34)

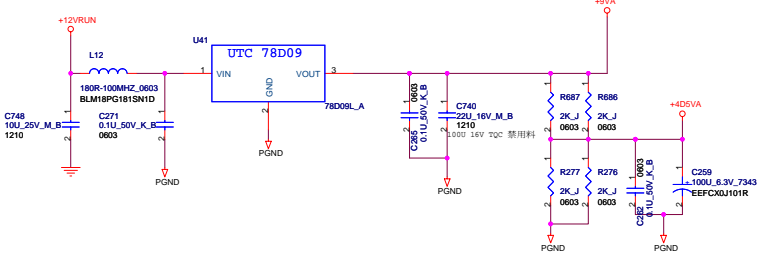
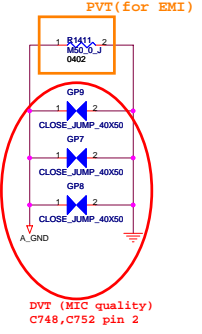
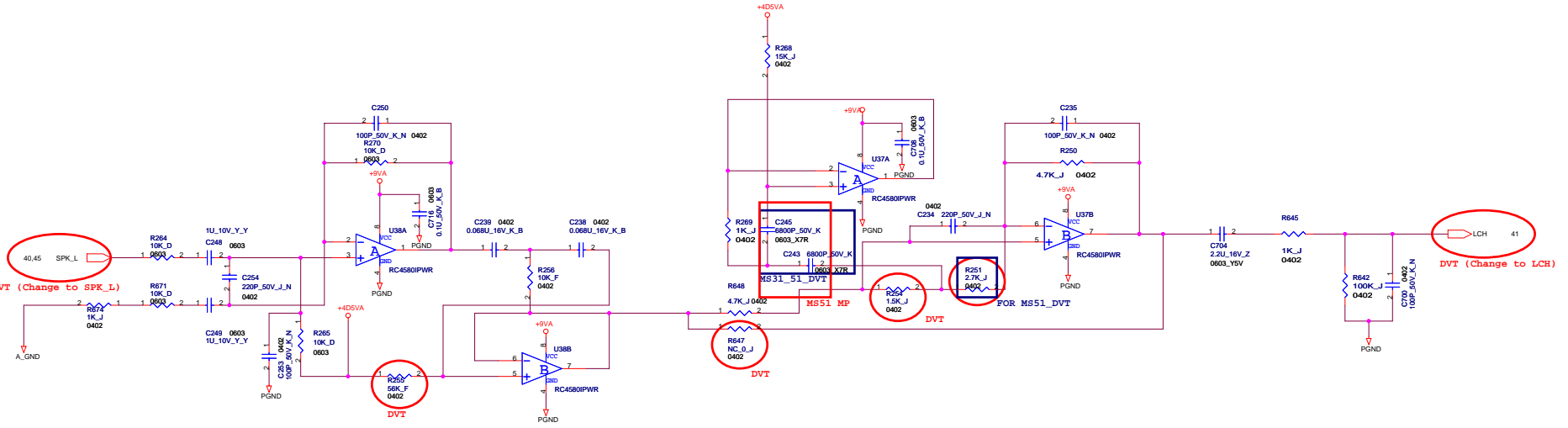
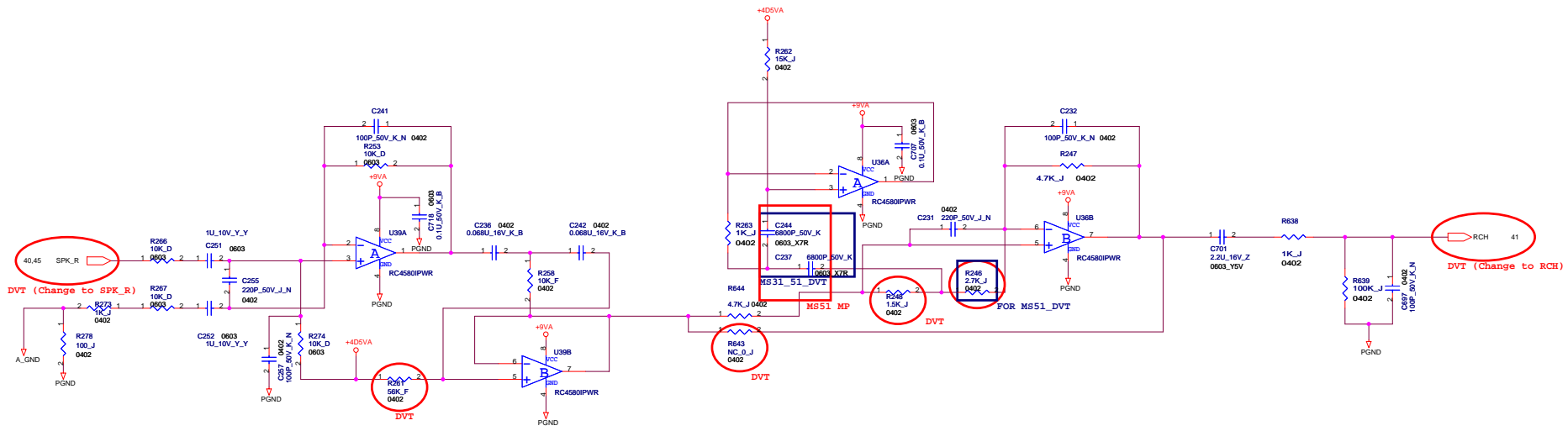


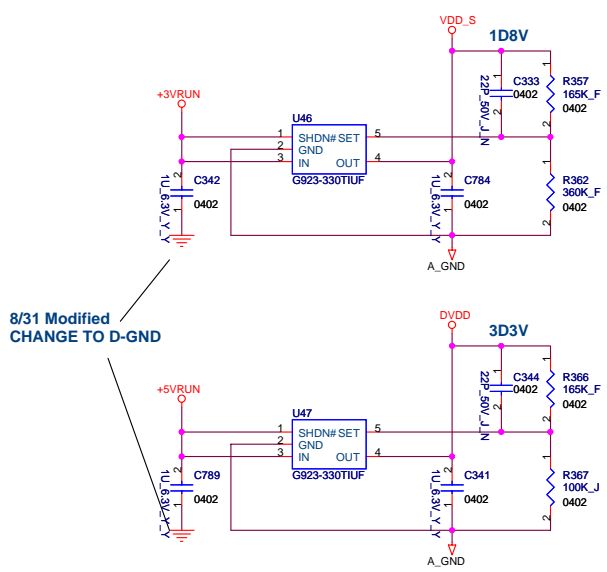
Int MIC amp circuit

FOXCONN HON HAI PRECISION IND. CO., LTD.		
CPBG - R&D Division		
Title	AUDIO(CODEC & POWER)	
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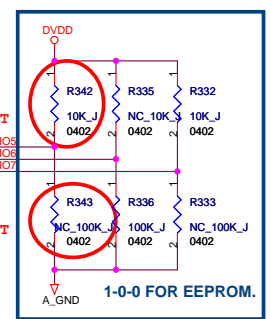






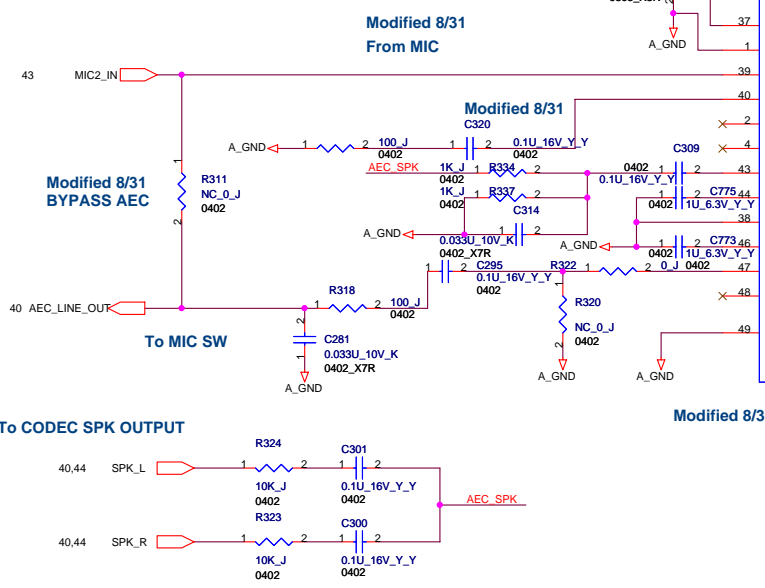
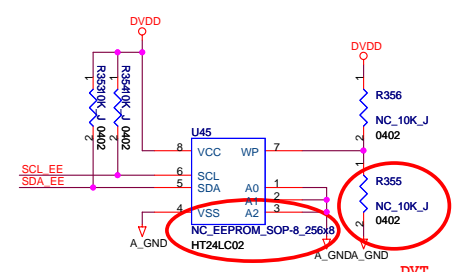
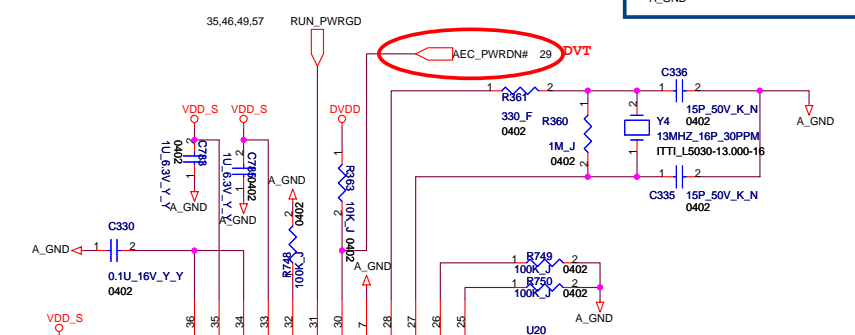


8/31 Modified
CHANGE TO D-GND

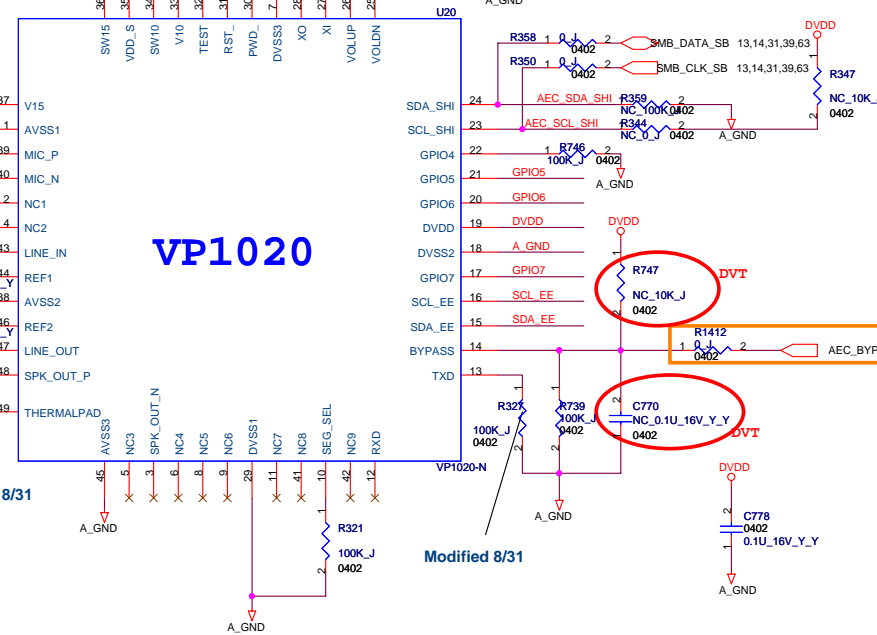


MODE	GPIO7	GPIO6	GPIO5
INTERNAL	0	0	X
RESERVED	0	1	X
EEPROM 256B	1	0	0
EEPROM 1KB	1	1	0
SHI	1	0	1
UART	1	1	1

8/31 Modified



VP1020

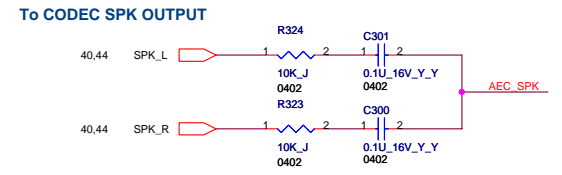


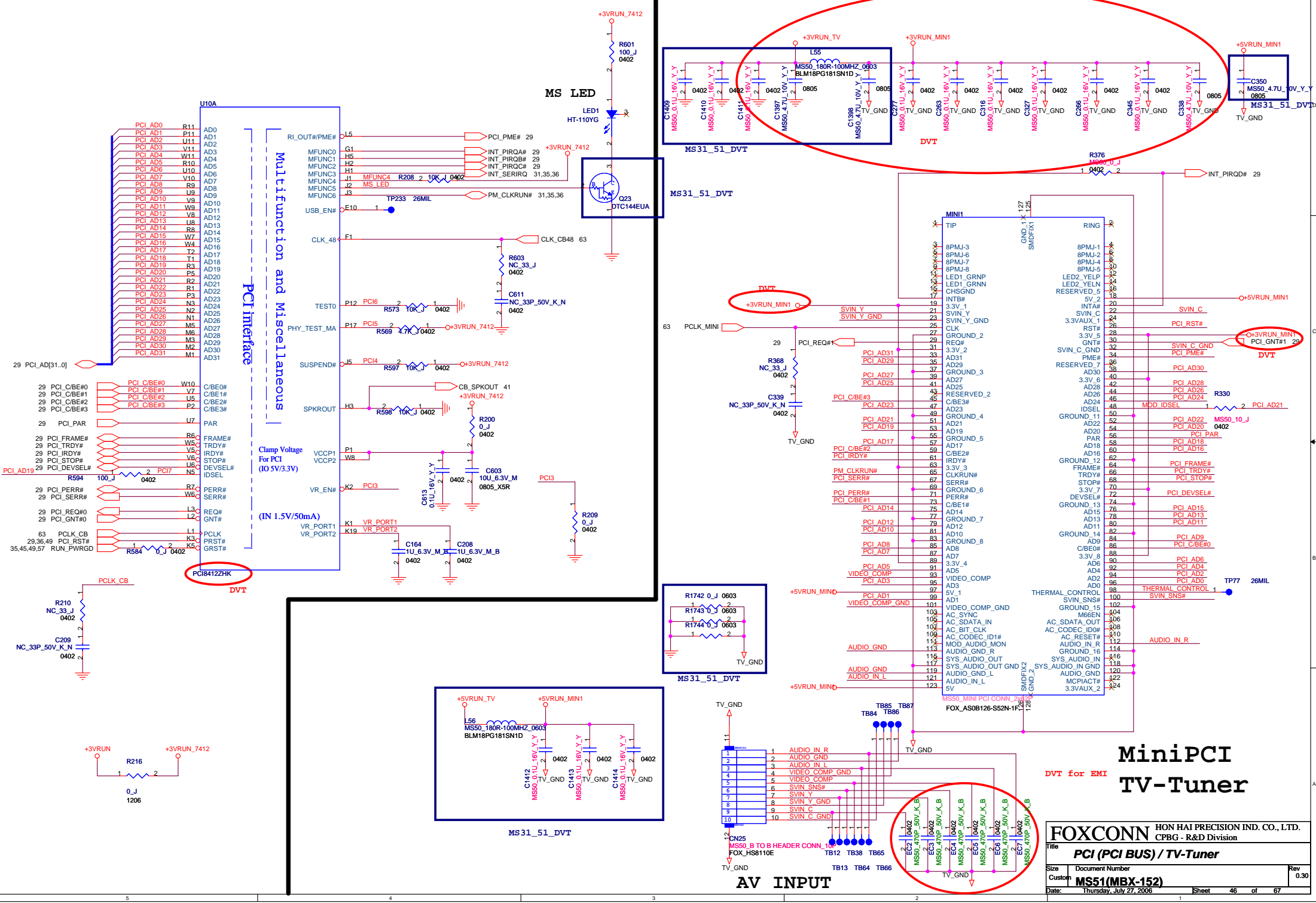
DVT

DVT



PVT



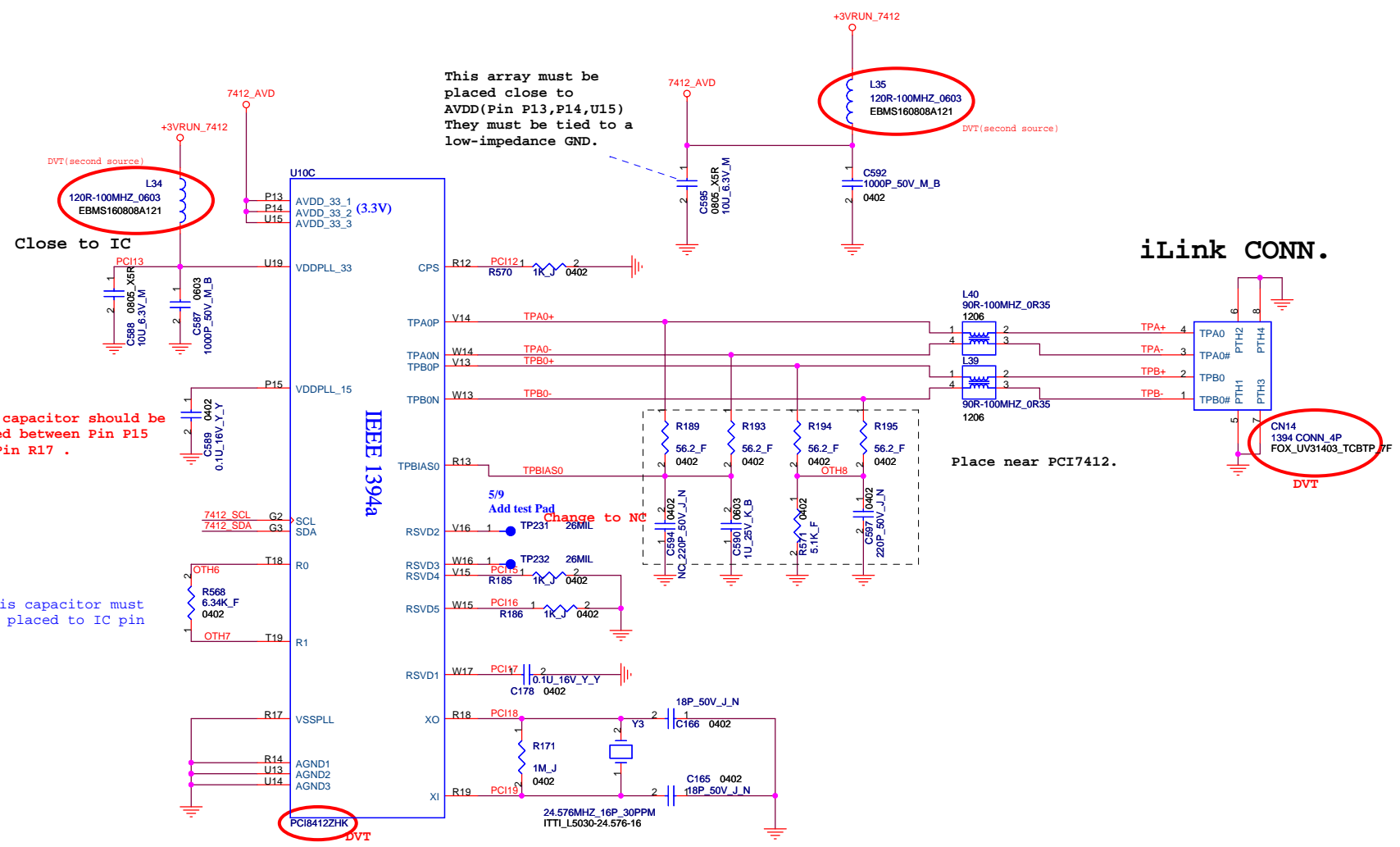


MiniPCI TV-Tuner

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **PCI (PCI BUS) / TV-Tuner**

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DVT(second source)
 L34
 120R-100MHZ_0603
 EBMS160808A121
 Close to IC

This array must be placed close to AVDD (Pin P13,P14,U15) They must be tied to a low-impedance GND.

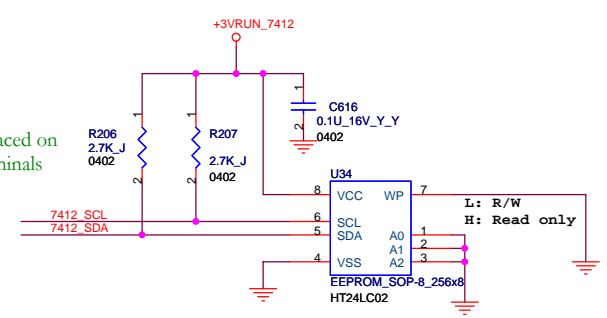
This capacitor should be placed between Pin P15 and Pin R17 .

This capacitor must be placed to IC pin

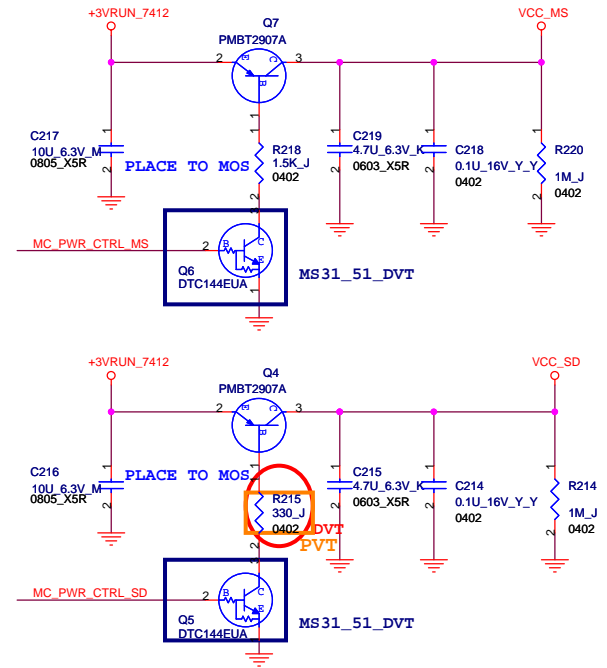
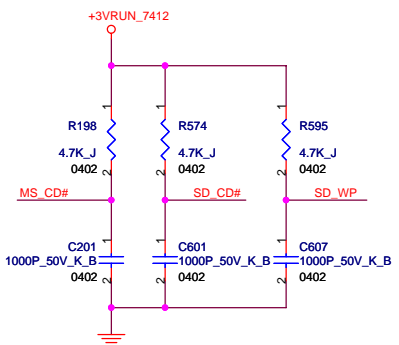
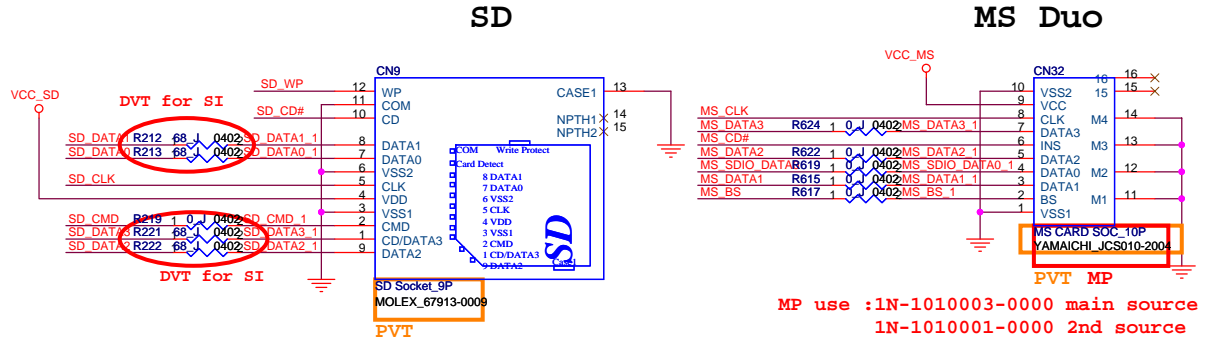
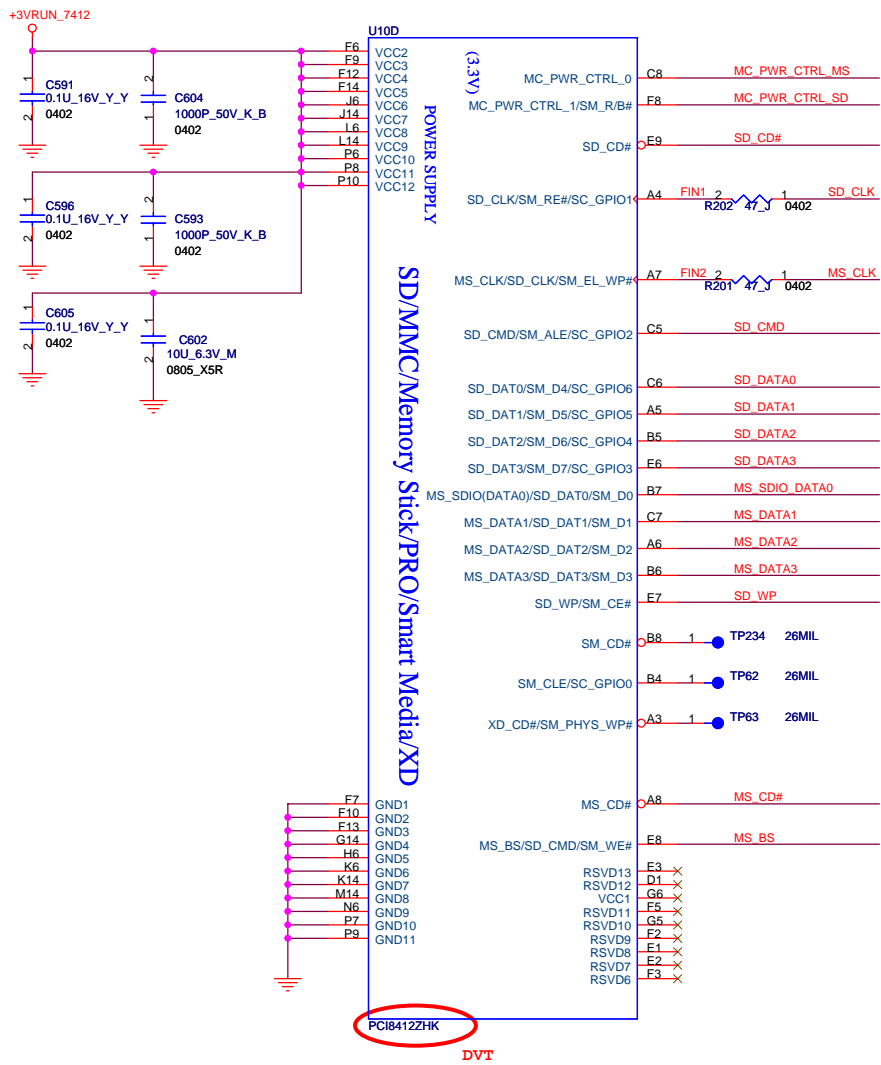
5/9 Add test Pad Change to NC

Place near PCI7412.

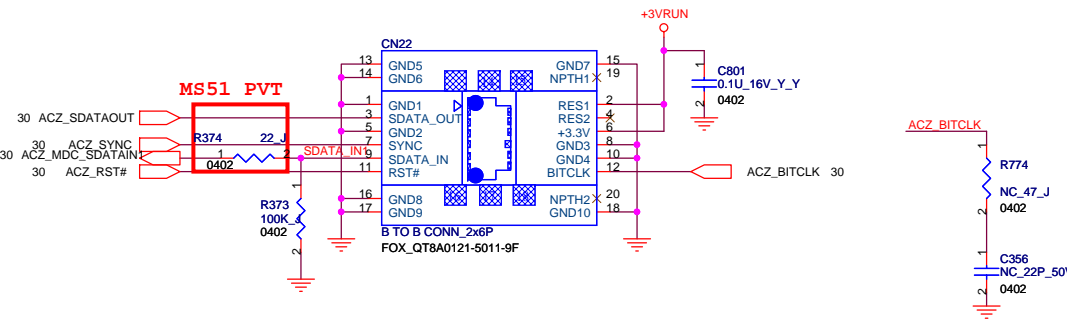
Resistors should be placed on the SCL and SDA terminals



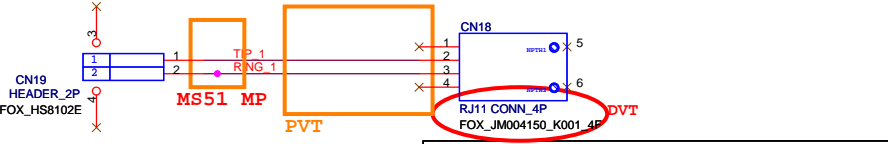
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CPBG - R&D Division	
Title	PCI (I LINK)
Size	Document Number
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MDC CONN.



RJ11 CONN.



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CPBG - R&D Division

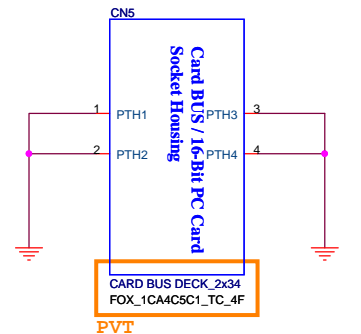
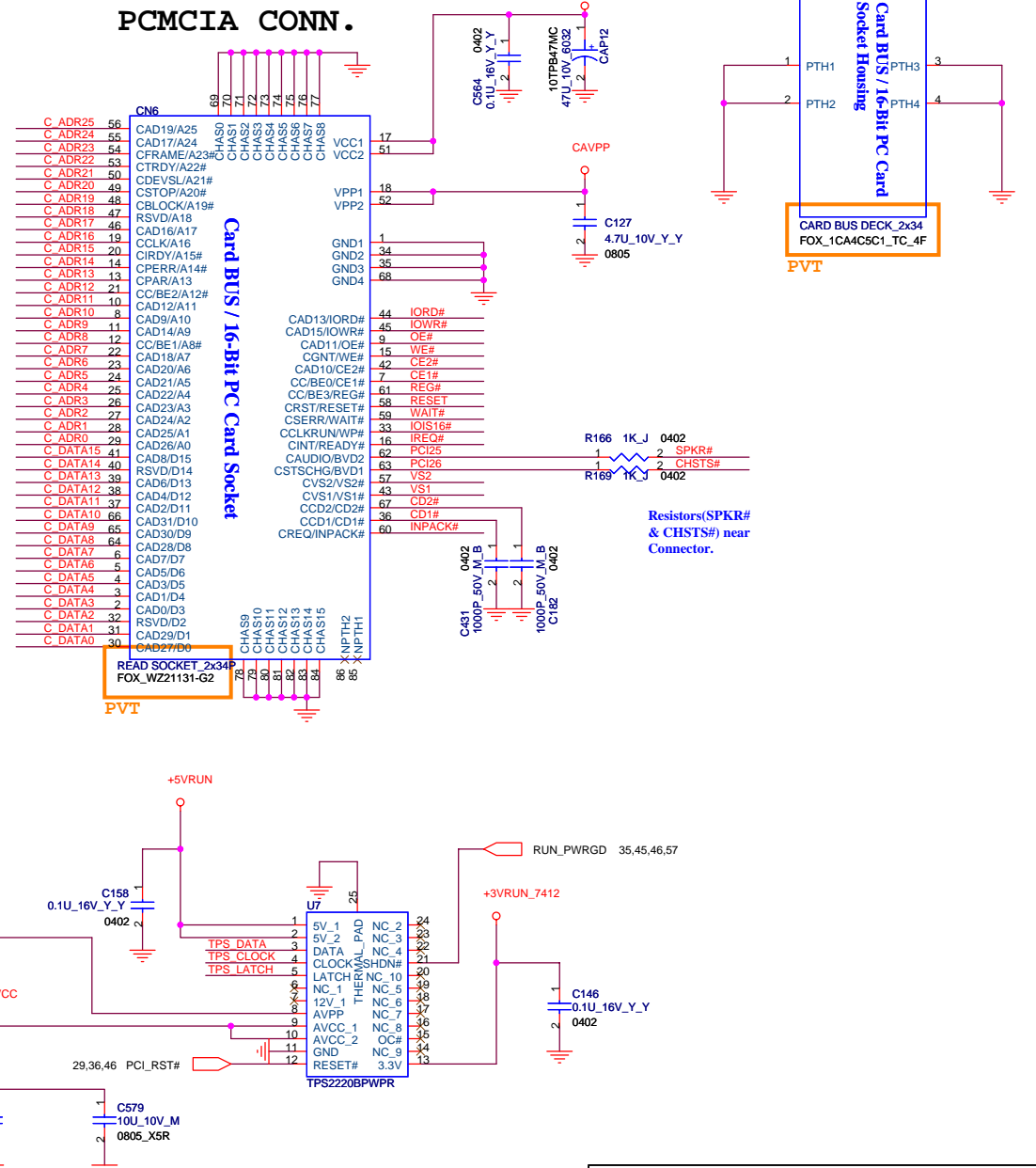
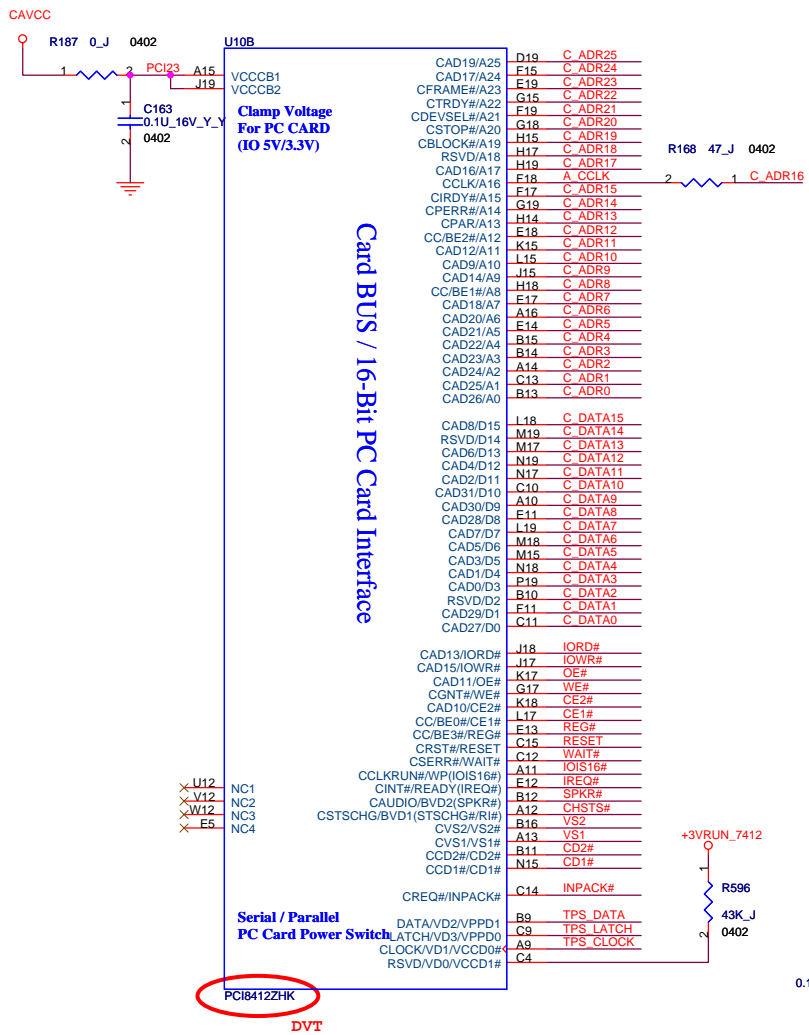
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Size: A3
Date: Thursday, July 27, 2006

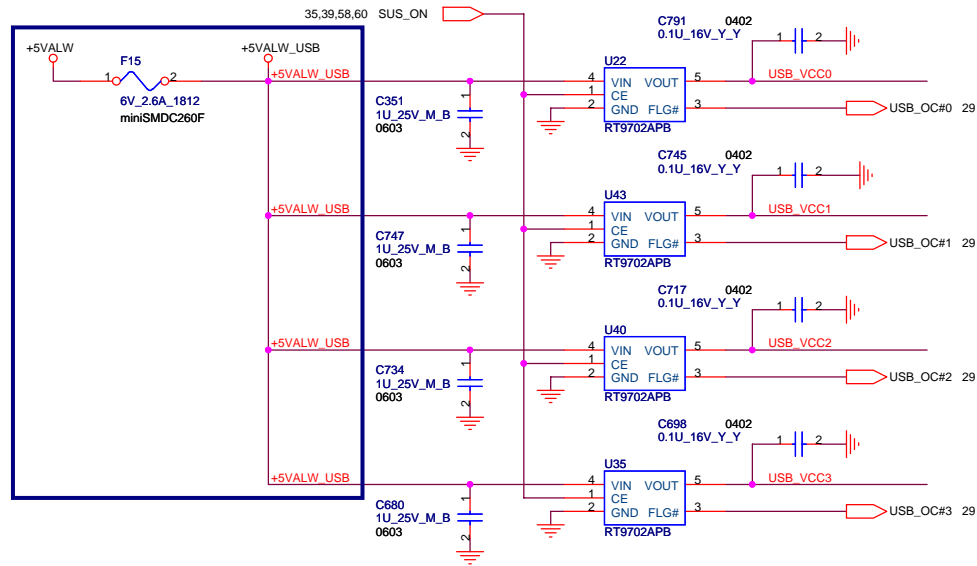
Document Number: **MS51(MBX-152)**

Rev: 0.30

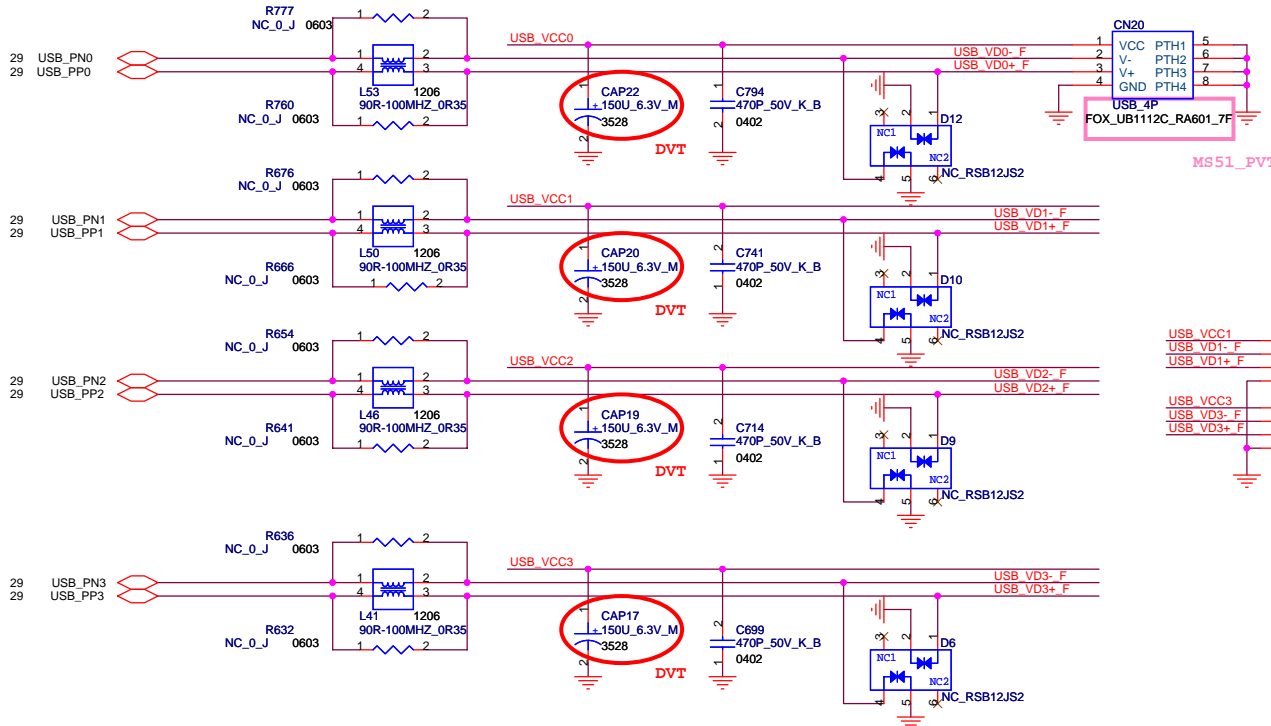
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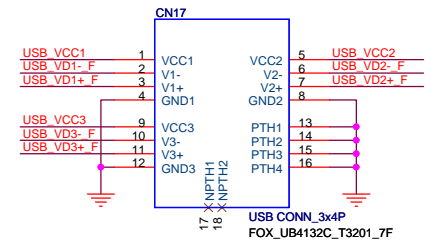
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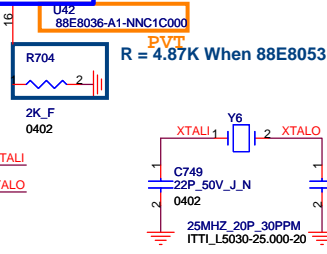
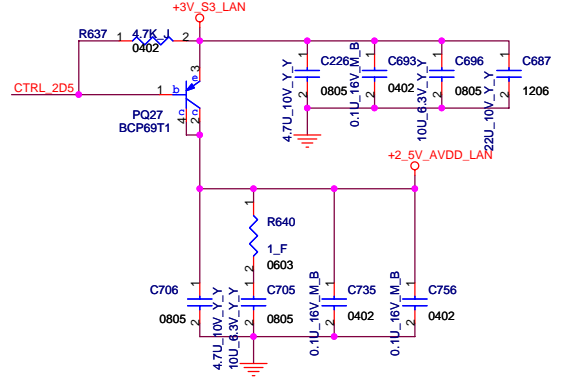
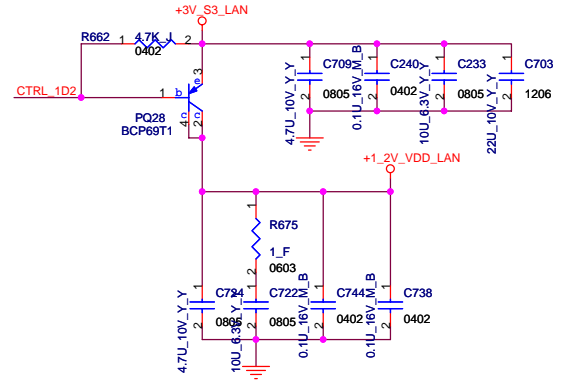
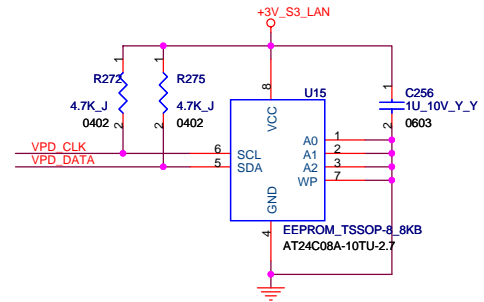
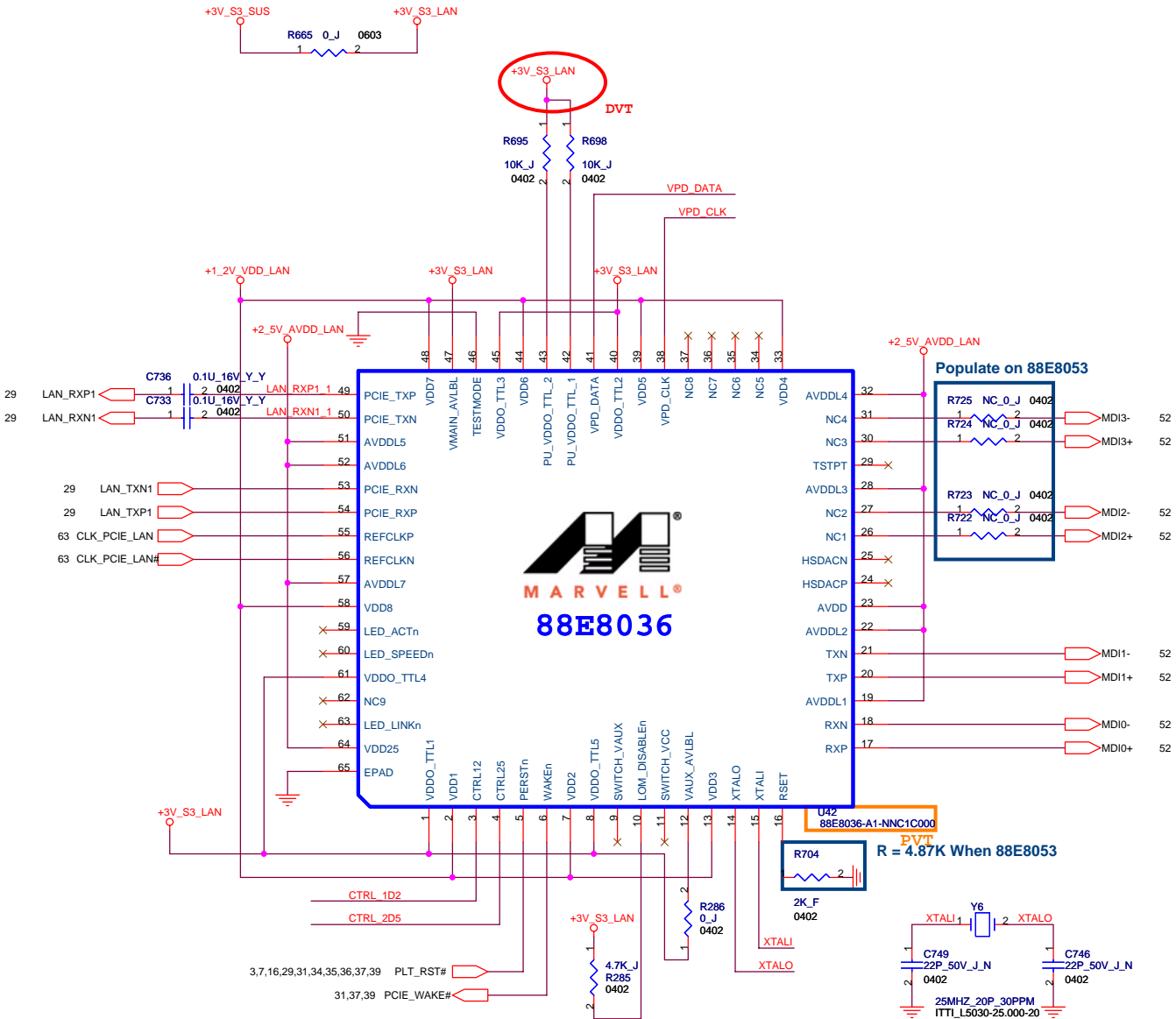


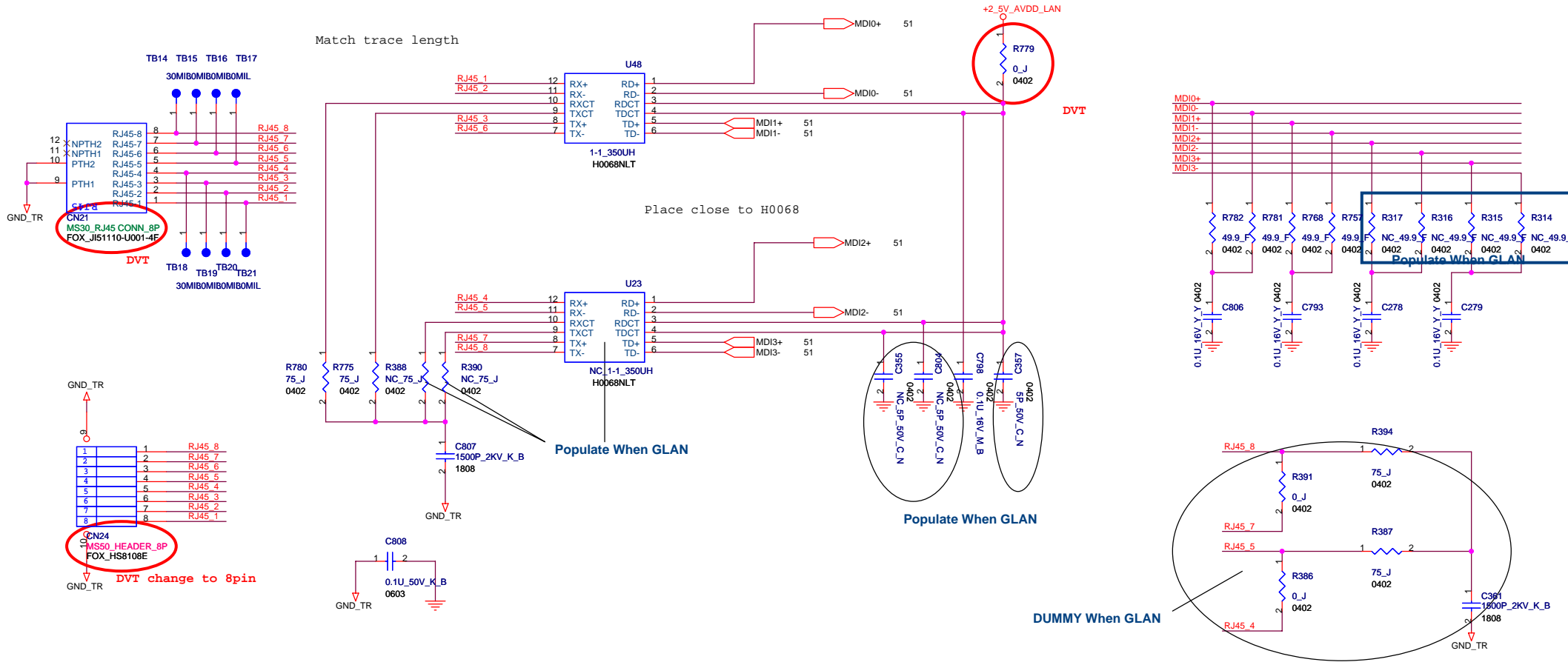
Use Power Switch

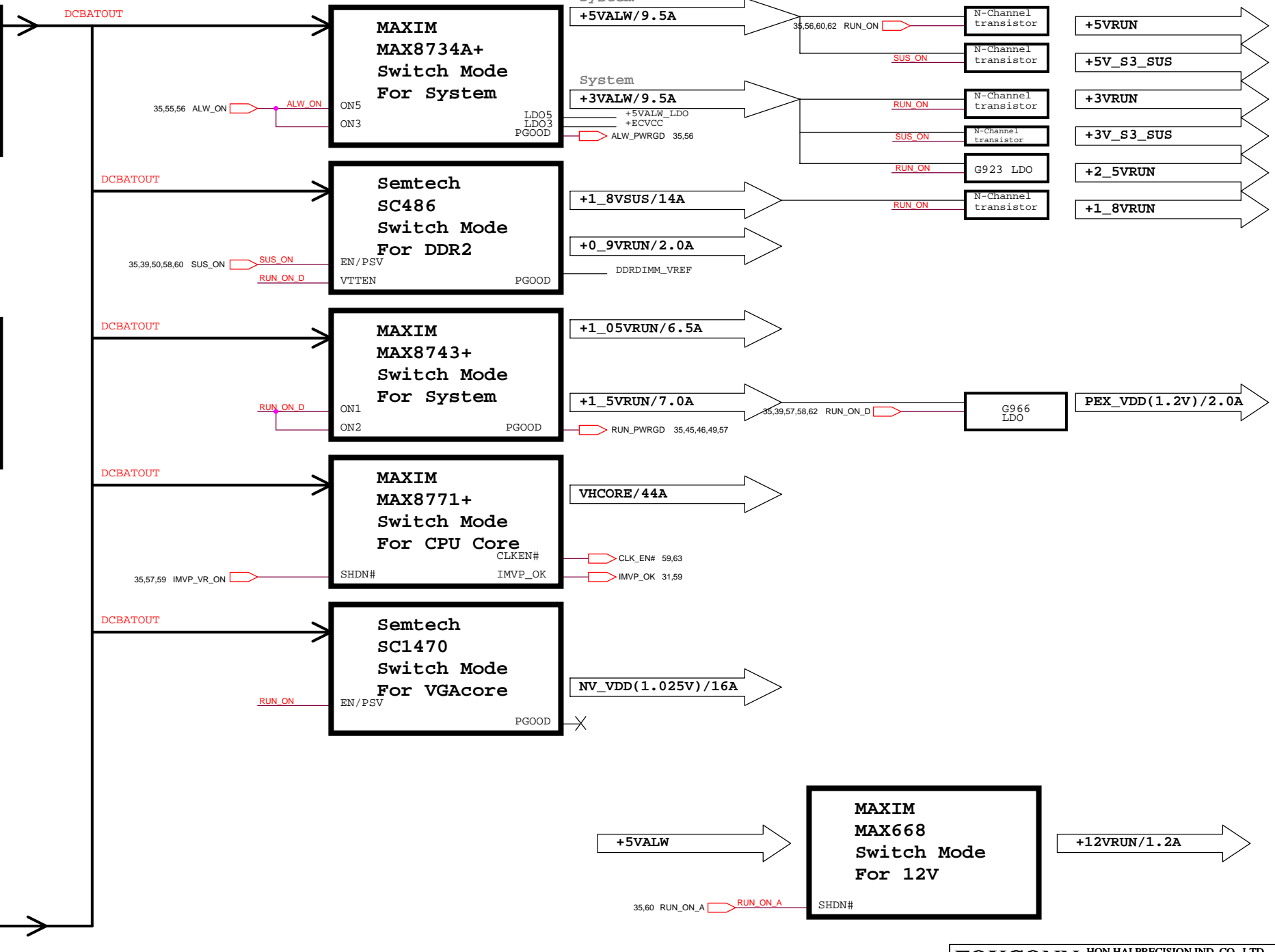
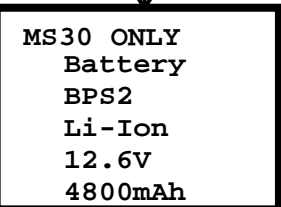
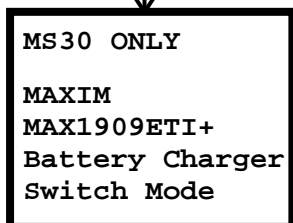
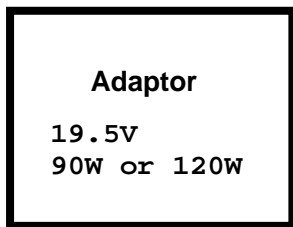


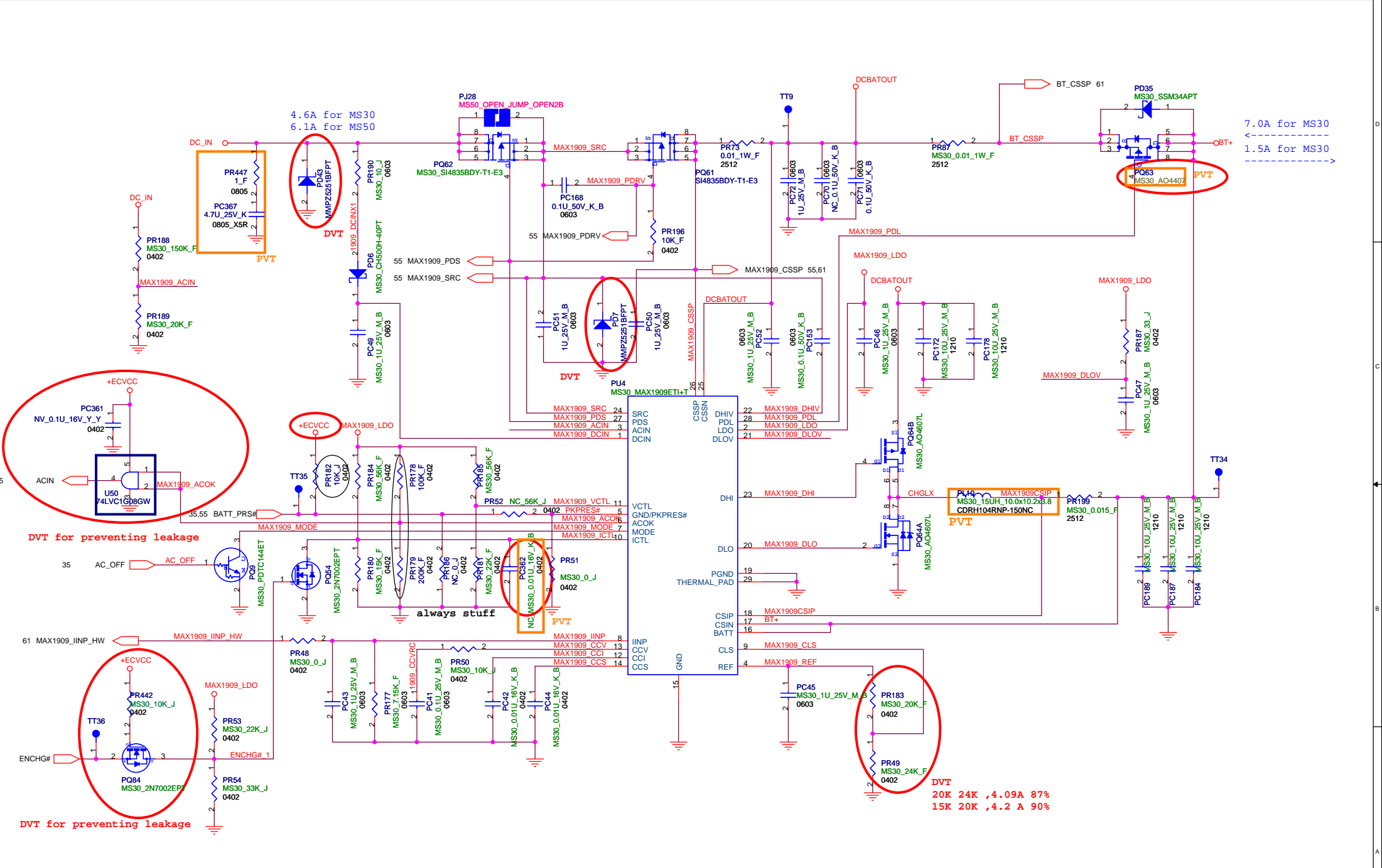
USB CONN X 4



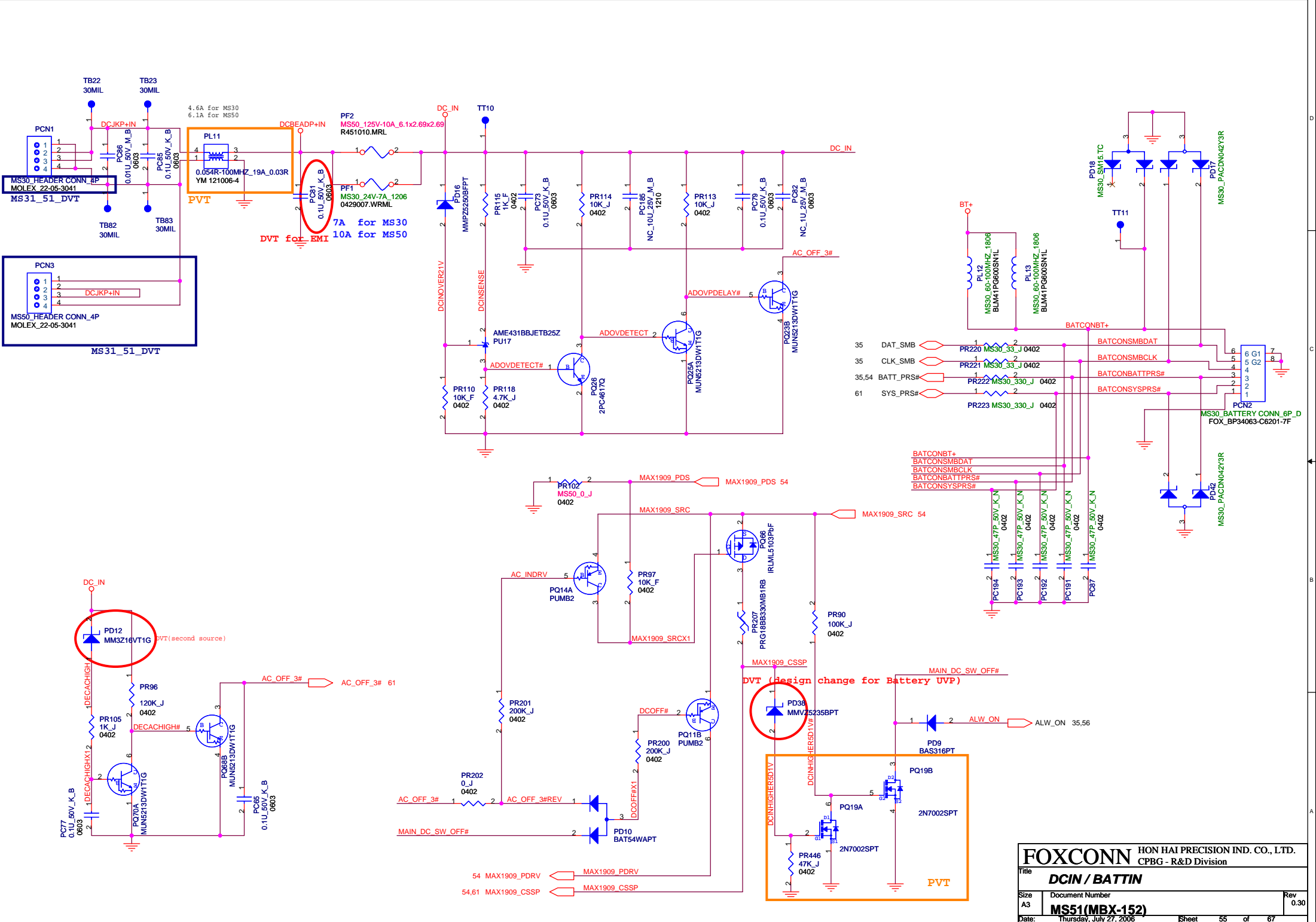




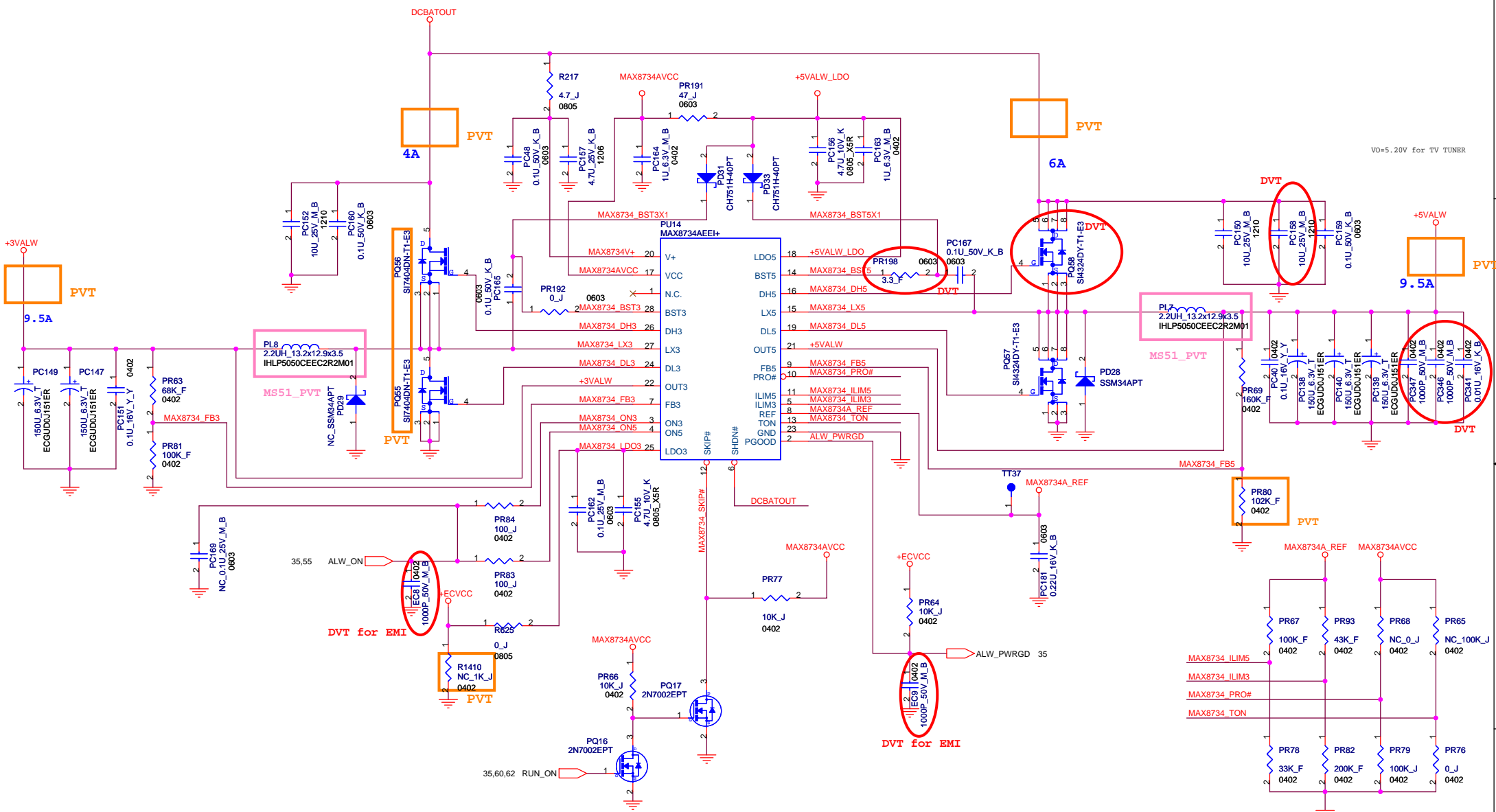




DVT
 20K 24K ,4.09A 87%
 15K 20K ,4.2 A 90%



FOXCONN		HON HAI PRECISION IND. CO., LTD.	
Title DCIN / BATTIN			
Size A3			
Date: Thursday, July 27, 2006		Sheet 55 of 67	
Document Number MS51(MBX-152)		Rev 0.30	

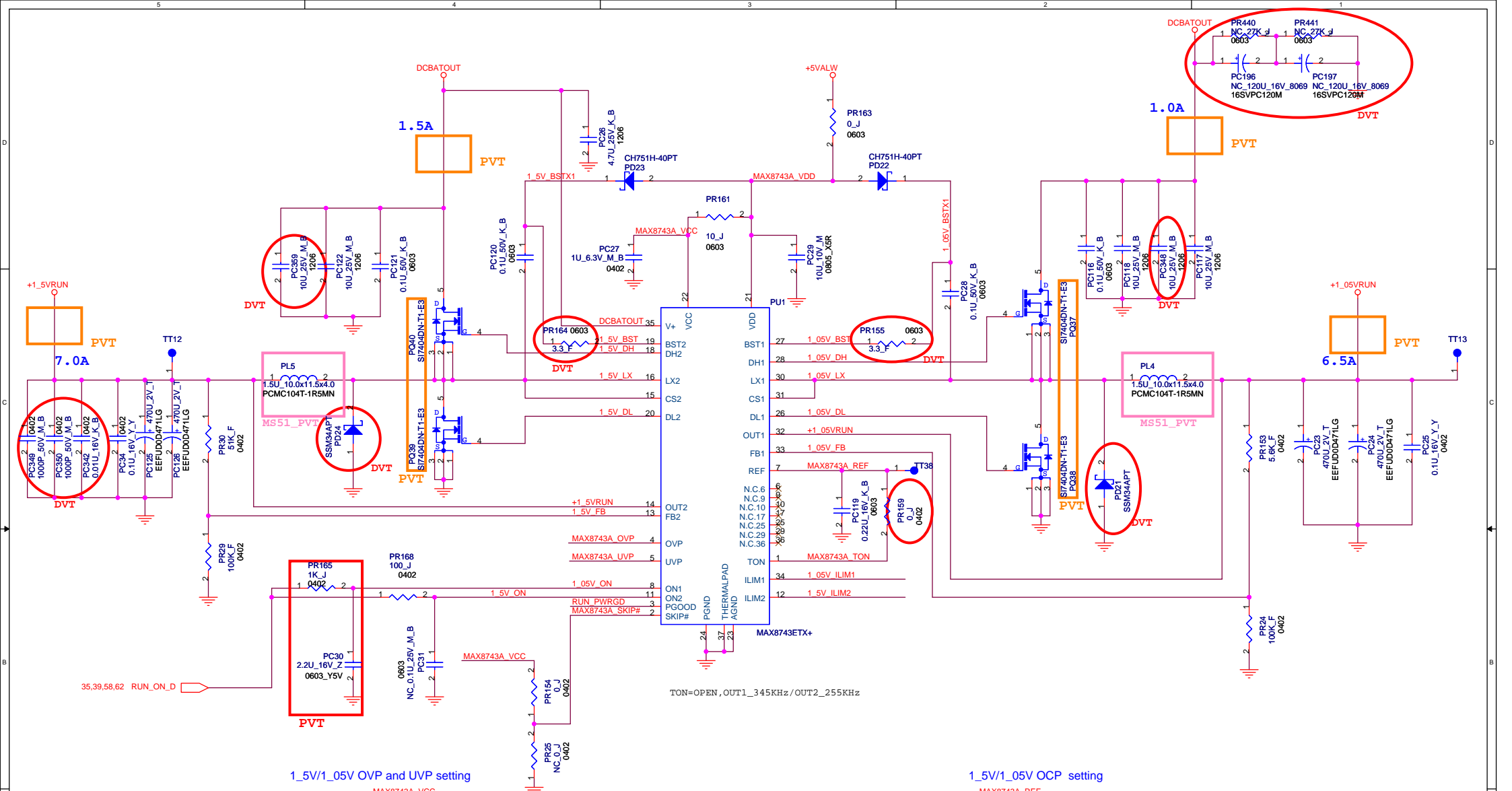


Vo=5.20V for TV TUNER

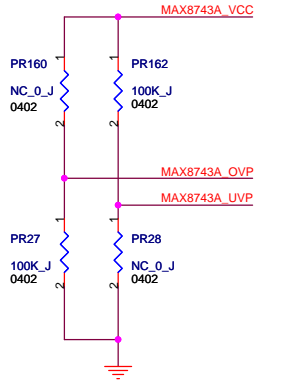
TON connect to GND = 5V/400KHZ, 3.3V/500KHZ

ILIM5/ILIM3 for setting OCP

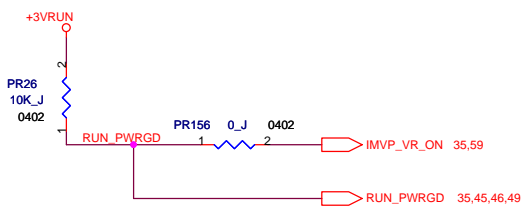
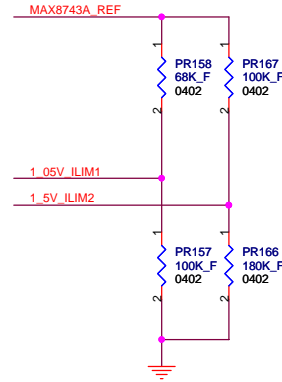
FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title SYS Power (3D3VALW/5VALW)		
Size A3	Document Number MS51(MBX-152)	Rev 0.30
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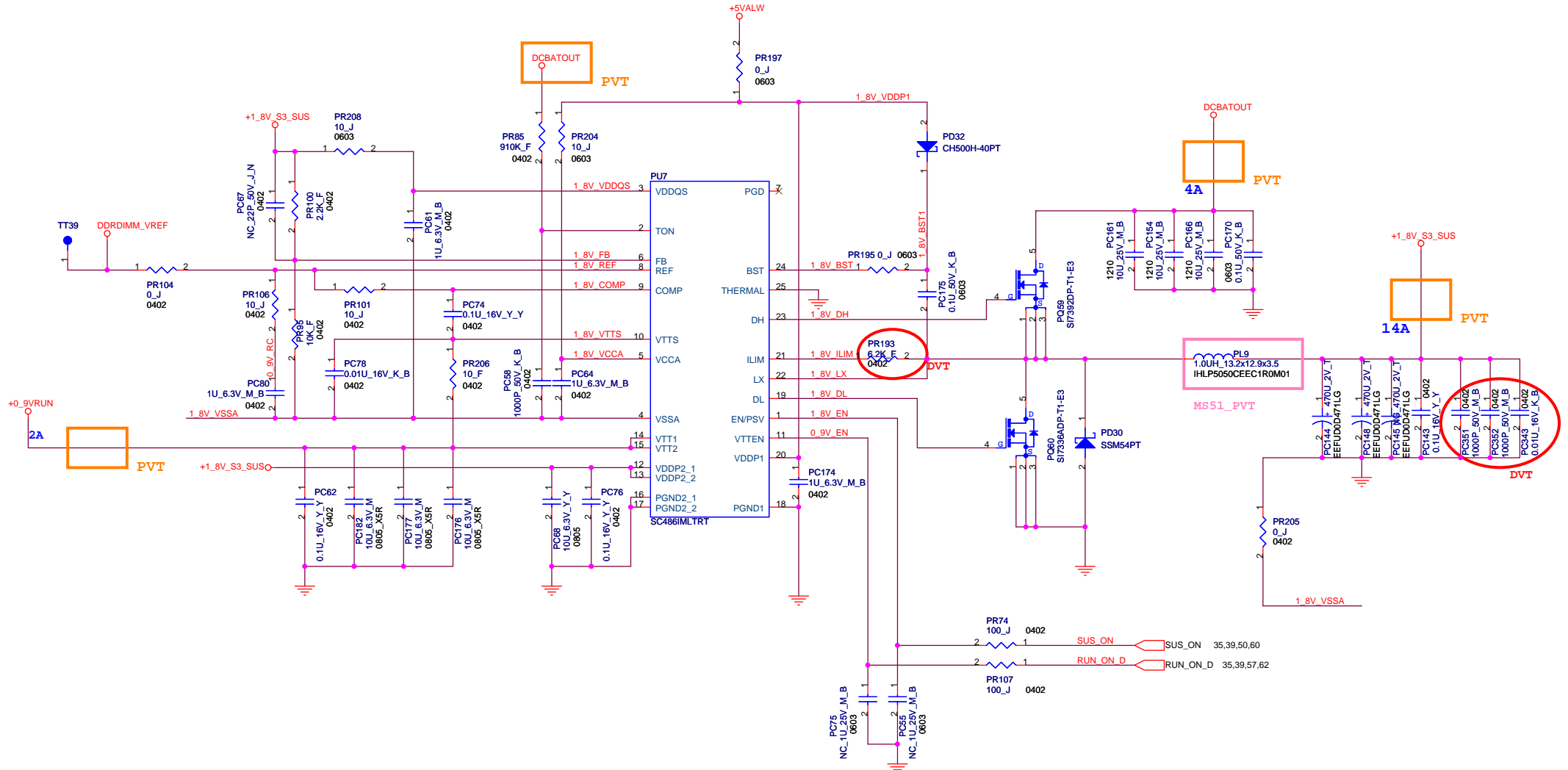


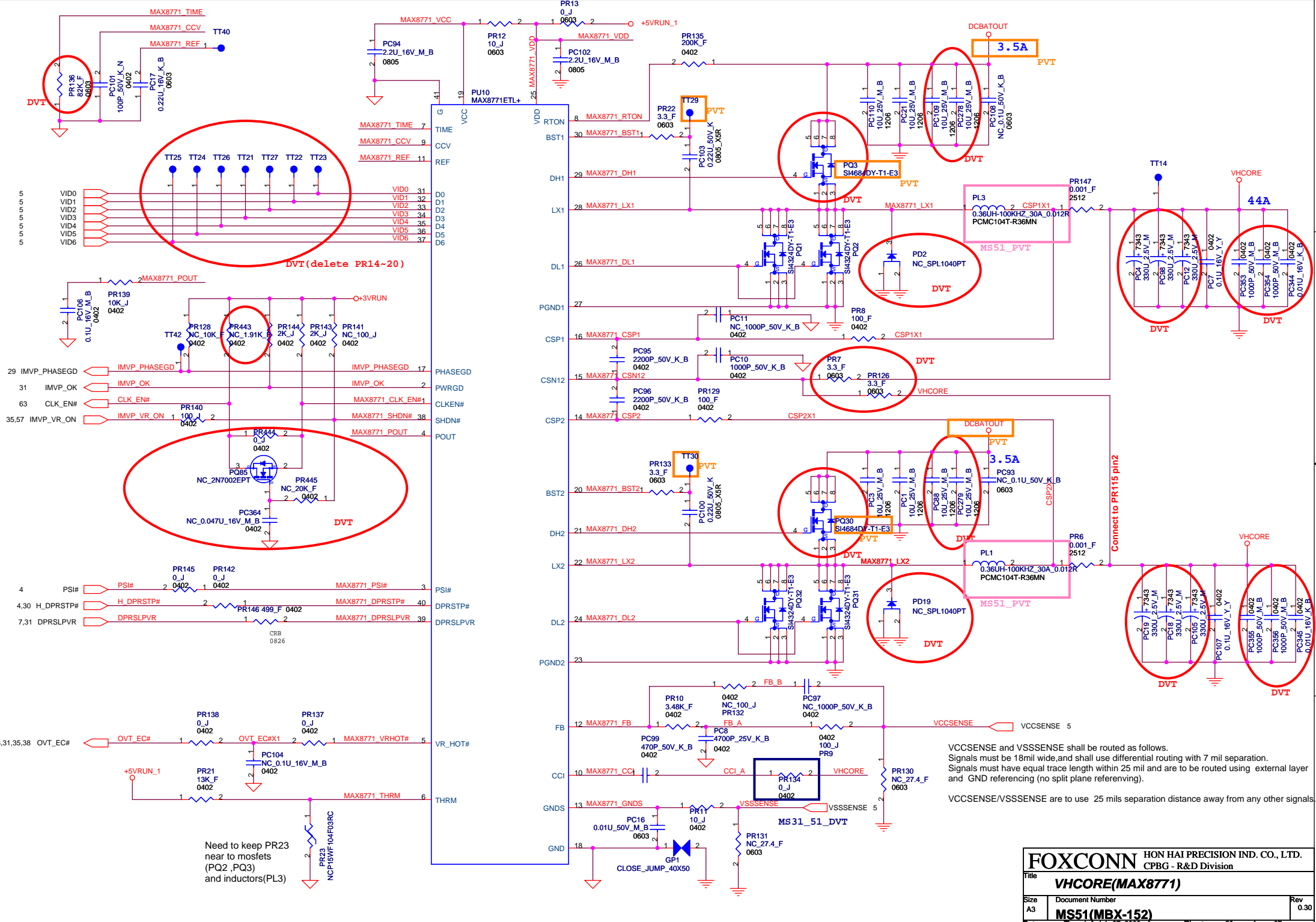
1.5V/1.05V OVP and UVP setting



1.5V/1.05V OCP setting



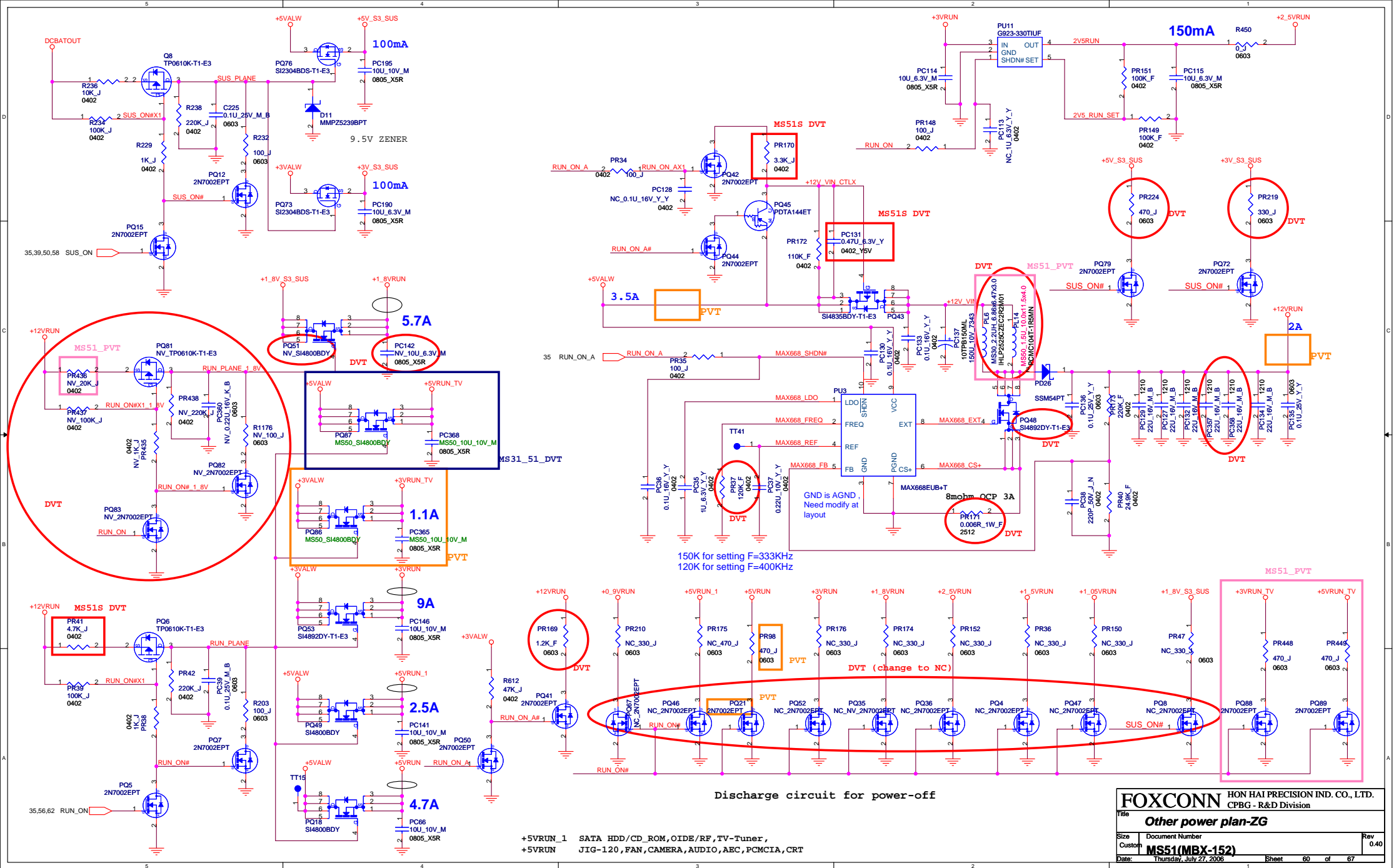




VCCSENSE and VSSSENSE shall be routed as follows.
 Signals must be 18mil wide, and shall use differential routing with 7 mil separation.
 Signals must have equal trace length within 25 mil and are to be routed using external layer and GND referencing (no split plane referencing).

VCCSENSE/VSSSENSE are to use 25 mils separation away from any other signals.

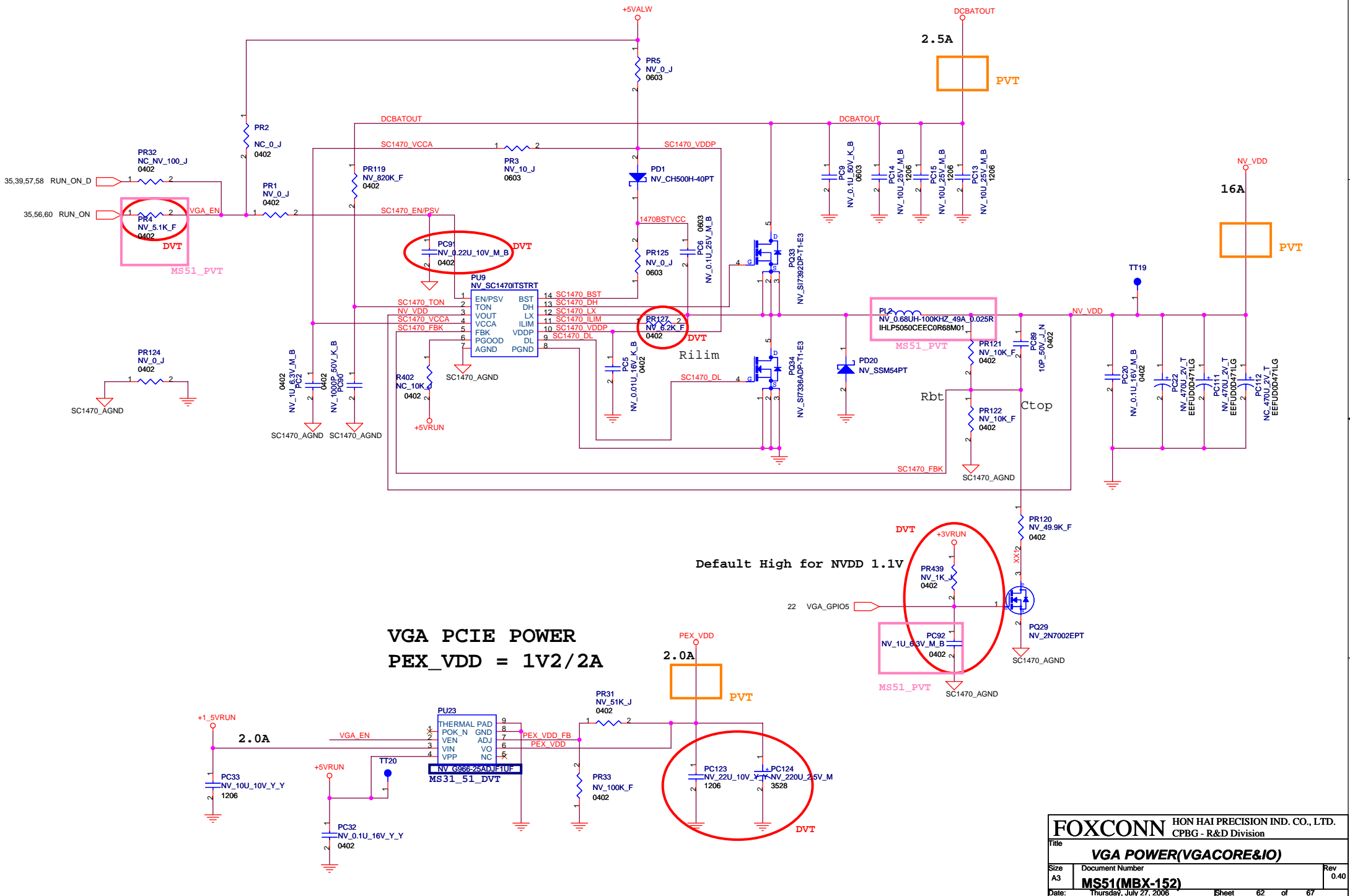
Need to keep PR23 near to mosfets (PQ2, PQ3) and inductors(PL3)

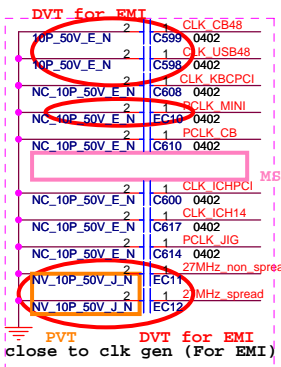


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CPBG - R&D Division

File: **Other power plan-ZG**

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PVT DVT for EMI close to clk gen (For EMI)

Length as short as possible.

PCLK_MINI DVT

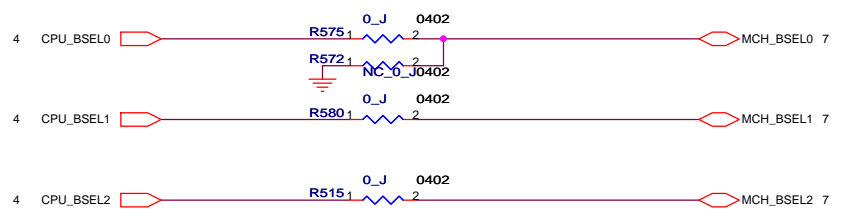
PCLK_MINI DVT

ICH7 DMI

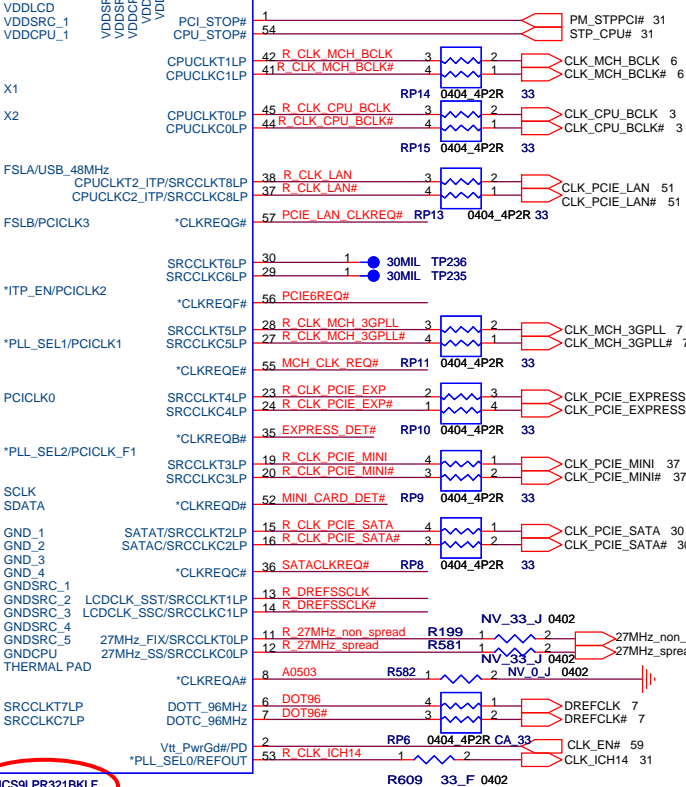
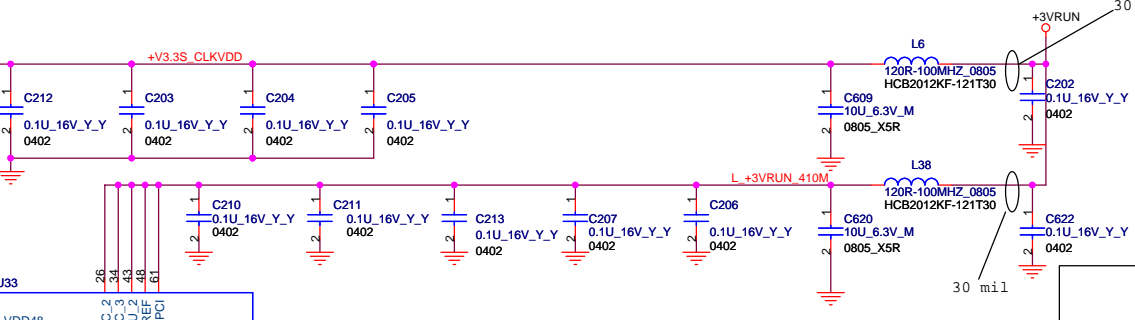
SM bus Address : 1101001 (ICH7) For clock generator

FSB Frequency Table:

FSLB	FSLA	CPU	SRC[7:0]	PCI
0	0	100	100	33
0	1	133	100	33
1	0	200	100	33
1	1	166	100	33



Pin	Pin 53/59/60/64	Value
pin53	pin 11/12	SRCLKL0
0		27MHz (v)
1		
pin59	pin 15/16	SRCLKL0
0		SATA (v)
1		
pin60	pin 37/38	SRCLKL8 (v)
0		CPU 2 ITP
1		
pin64	pin 13/14	LCDCLK_SS (CA)
0		SRCLKL1 (NV)
1		



CALISTOGA Chip HOST

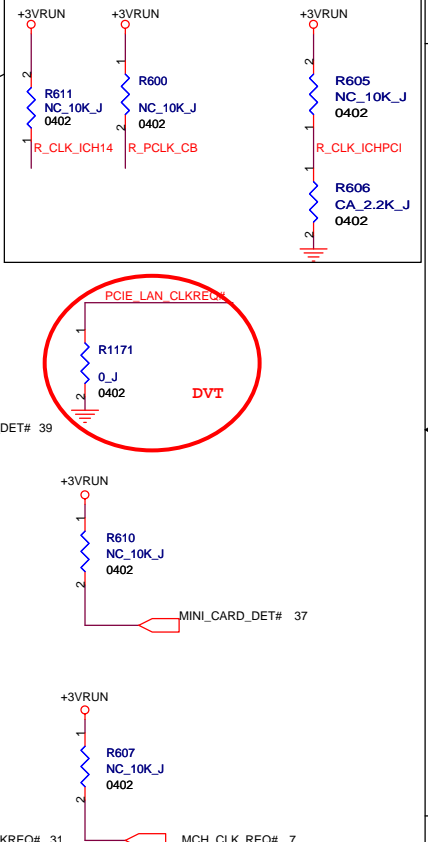
CPU

pin53/59/60/64 with internal pull-up resistor
No Stuff Pull-up Resistor (R1125, R1124, R49)
If EVT ok, del them in DVT
R1021/R48 changed to 2.2Kohm

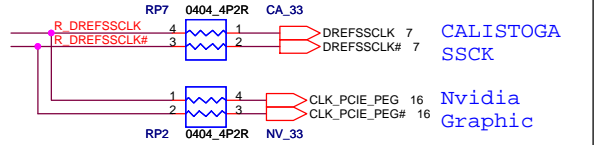
ICH7M SATA

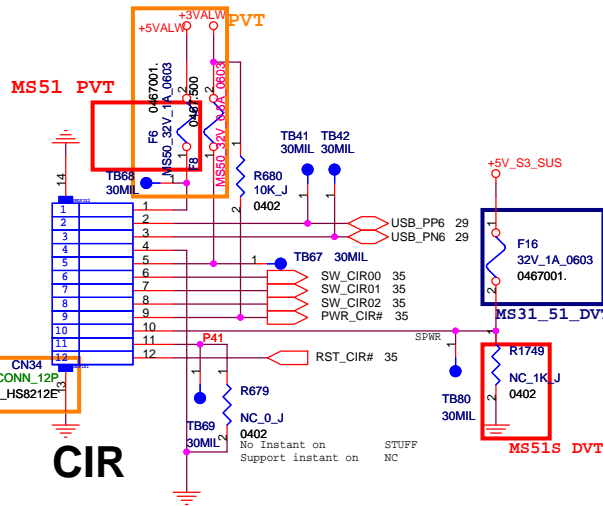
Nvidia Graphic

CALISTOGA DOT96

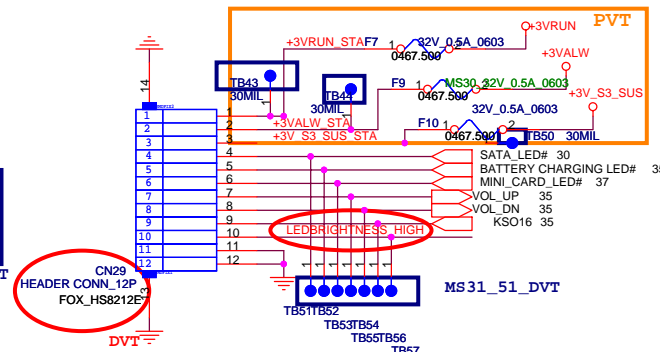


CLKREQ with internal pull-up resistor
No Stuff Pull-up Resistor (R69, R40, R41, R70, R1126, R1127)
If EVT ok, del them in DVT

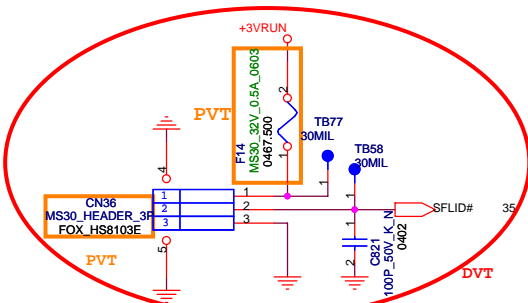
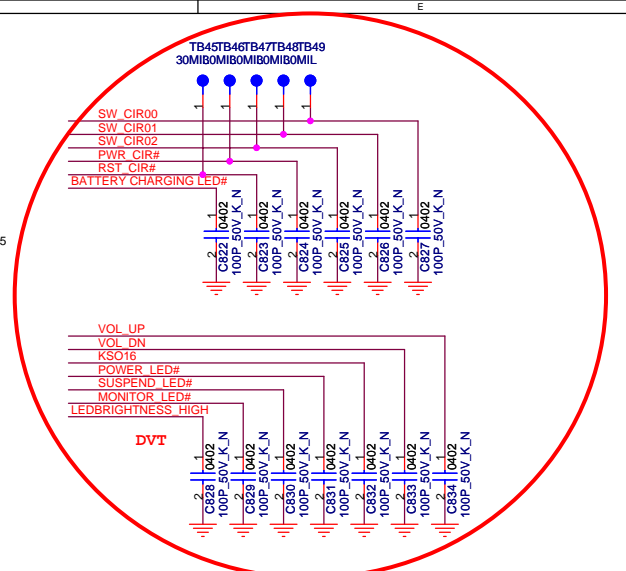




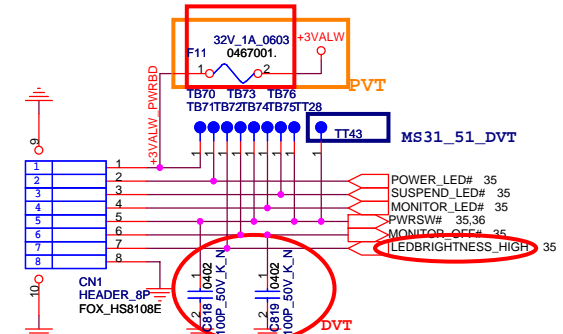
CIR



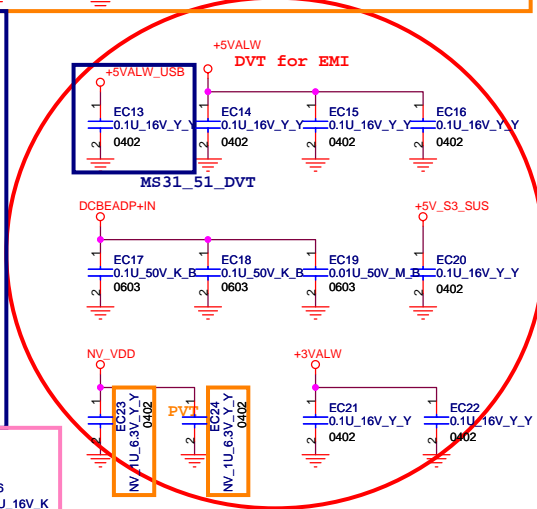
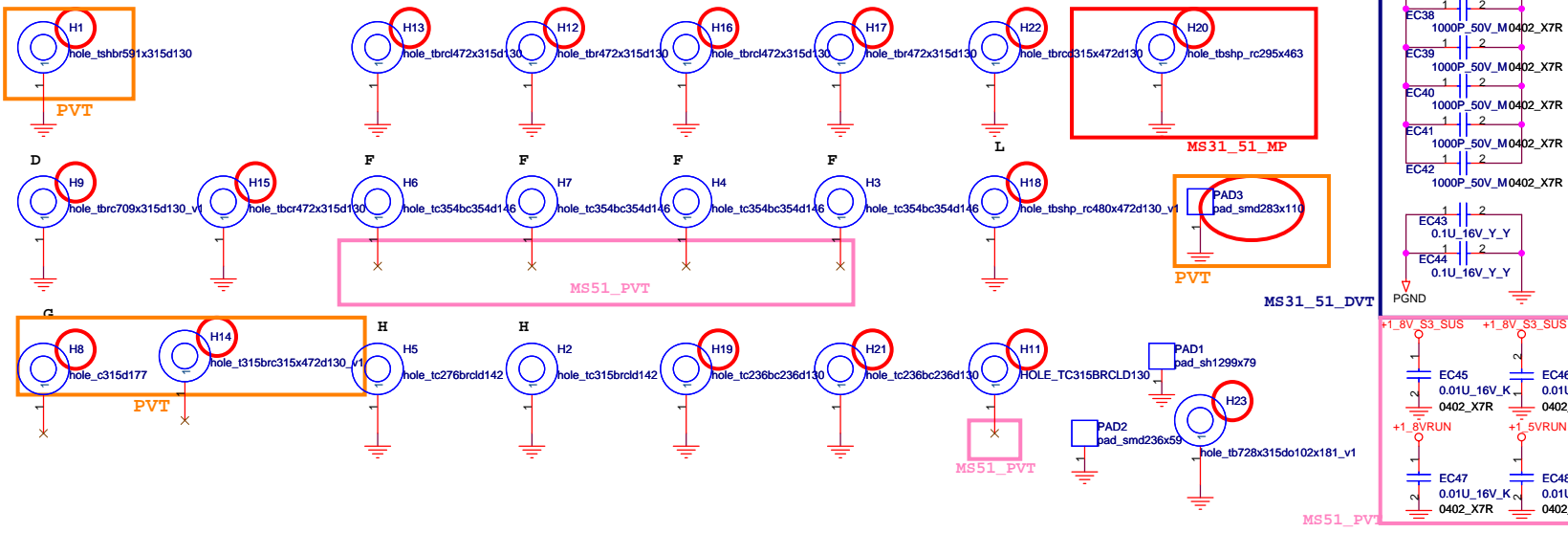
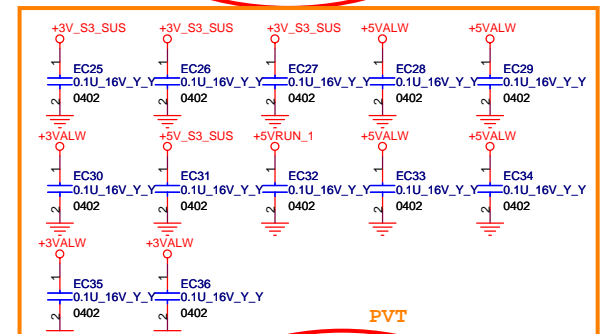
STATUS LED CONN

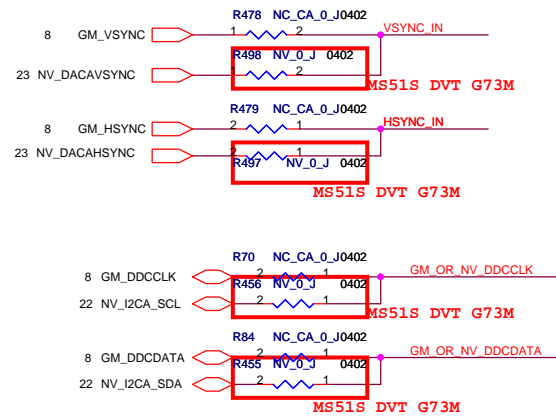
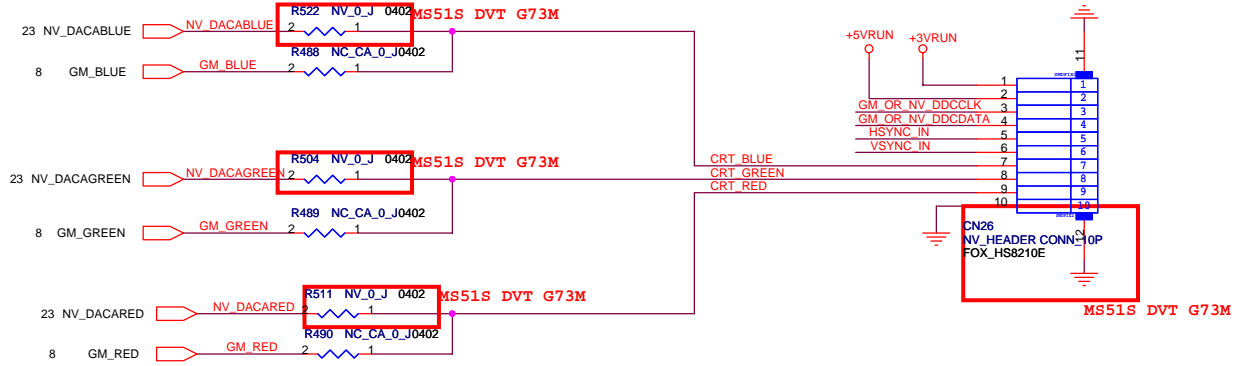


Cover SW CONN



Power LED/Power BTN





9/29 Add CN11 signal for both QTD8 (R6_30) and RP(R6_50) to...

9/6 Power

9/7 Power

9/8 Power

9/9 Power

9/10 Power

9/11 Power

9/12 Power

9/13 Power

9/14 Power

9/15 Power

9/16 Power

9/17 Power

9/18 Power

9/19 Power

9/20 Power

9/21 Power

9/22 Power

9/23 Power

9/24 Power

9/25 Power

9/26 Power

9/27 Power

9/28 Power

9/29 Power

9/30 Power

9/31 Power

9/32 Power

9/33 Power

9/34 Power

9/35 Power

9/36 Power

9/37 Power

9/38 Power

9/39 Power

9/40 Power

9/41 Power

9/42 Power

9/43 Power

9/44 Power

9/45 Power

9/46 Power

9/47 Power

9/48 Power

9/49 Power

9/50 Power

9/51 Power

9/52 Power

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9/67 Power

9/68 Power

9/69 Power

9/70 Power

9/71 Power

9/72 Power

9/73 Power

9/74 Power

9/75 Power

9/76 Power

9/77 Power

9/78 Power

9/79 Power

9/80 Power

9/81 Power

9/82 Power

9/83 Power

9/84 Power

9/85 Power

9/86 Power

9/87 Power

9/88 Power

9/89 Power

9/90 Power

9/91 Power

9/92 Power

9/93 Power

9/94 Power

9/95 Power

9/96 Power

9/97 Power

9/98 Power

9/99 Power

9/100 Power

